Wafer-Level Reliability Tests of InGaP HBTs Using High Current Stress

Frank H.F. Chau, Chien-Ping Lee*, Clarence Dunnrowicz and Barry Lin

EiC Corporation, 45738 Northport Loop West, Fremont, CA 94538, USA
Tel: (510) 979-8943, fax: (510) 979-8901, email: fchau@eiccorp.com
* Permanent Address: Dept. of Electronics Engineering, National Chiao Tung University, 1001 Ta Hsueh, Hsinchu, Taiwan

ABSTRACT

Current densities ranging from 440 to 543 kA/cm^2 were applied to InGaP HBTs in WLR tests. Even with such a high current stress at 440 kA/cm^2 and an estimated junction temperature of 396 °C, the transistor lasted for 101 hours before our failure criterion was met. The current gain degradation behavior was similar to that shown in traditional, low current reliability tests, namely a long, relatively stable or slow gradual degradation region after the initial stabilization took place, followed by a sudden, rapid gain degradation phase that led to device failure. The failure, however, was characterized by "1*kT*" current increase in the base current, in contrast to the "2*kT*" current increase at a much lower current density of 50 kA/cm^2 in traditional reliability tests. A mixed failure mode was observed at 75 kA/cm^2 stress current density. It is believed that biasing HBTs much beyond base pushout regime results in defect generation deep in the base through REDR associated with increased neutral base recombination. It is further supported by the fact that the lifetime of transistor appears to depend more on the applied base current, and not so much on the collector current density and junction temperature. WLR tests at extremely high current densities cannot replace traditional low current stress tests to predict HBT lifetime under the normal "use" conditions.

INTRODUCTION

Wafer-level reliability (WLR) test, if it can be done, is always attractive because one can complete the test in a much shorter time than traditional reliability test and even before wafer processing is fully completed. In the last ManTech conference, one group reported the use of a high current density up to 150 kA/cm^2 on InGaP HBTs and claimed to see a direct correlation between the WLR and long-term reliability test results through similar failure mechanism [1]. We have performed WLR tests on our InGaP HBTs under extremely high current stress from 440 kA/cm^2 up to 543 kA/cm^2 in an attempt to understand two issues associated with wafer-level reliability testing: (1) How high can the current density be pushed beyond the base pushout regime and still yield a direct correlation between room-temperature WLR and traditional low-current reliability test results at elevated ambient temperatures? (2) With increased neutral base recombination associated with Kirk effect, does the base current play a more important role than the collector current in WLR testing?

WLR TESTING

Our 2 × 6 μm^2 InGaP HBTs were fabricated in house. We initially attempted to use current densities such as 150 kA/cm^2 as in [1], then 200 and 300 kA/cm^2 on the devices, but did not see much degradation at all at these stress conditions. Current densities ranging from 440 to 543 kA/cm^2 were then used in the WLR stress tests, and represented 10 to 50 times the normal operation current densities used in our products. The collector voltage was limited to no more than 2.3 V to avoid junction breakdown. Under such high current densities, the devices were well into the base pushout regime. But even so, they still had reasonable current gains above 30. In our HBTs, the critical current for the onset of Kirk effect is about 40 kA/cm^2. The junction temperatures were estimated based on a thermal resistance of 3000 °C/W. The lifetime was defined as the point when the peak room-temperature current gain dropped by 30% from its initial value before stabilization took place.

Table I shows the junction temperatures and lifetimes obtained in the InGaP HBTs biased at different stress conditions.

TABLE I
Lifetimes of InGaP HBTs biased at different WLR stress conditions

Wafer	Tx.	Ic	Vce	Ib	Current Density	Power Density	Junction Temperature	Lifetime
I	A	52.8 mA	2.3 V	1.0 mA	440 kA/cm^2	1.02 MW/cm^2	396 °C	101.0 Hrs
	B	56.2 mA	2.3 V	1.3 mA	468 kA/cm^2	1.09 MW/cm^2	421 °C	17.9 Hrs
	C	60.1 mA	2.0 V	1.3 mA	501 kA/cm^2	1.02 MW/cm^2	394 °C	17.4 Hrs
	D	57.8 mA	2.3 V	1.5 mA	482 kA/cm^2	1.13 MW/cm^2	433 °C	8.0 Hrs
II	E	60.0 mA	2.3 V	1.5 mA	500 kA/cm^2	1.17 MW/cm^2	448 °C	8.0 Hrs
	F	65.0 mA	2.3 V	2.1 mA	543 kA/cm^2	1.28 MW/cm^2	486 °C	2.3 Hrs

The gummel plots of Transistor A measured at different stages of stress are shown in Fig. 1. The transistor stabilized after about 20 minutes of current stress, and then remained relatively stable for the next 100 hours. After about 100.9 hours of stress, the transistor then suddenly went into a rapid gain degradation phase similar to that reported in Refs. [1] and [2]. Within the next 23 minutes of stress, the failure criterion was met.

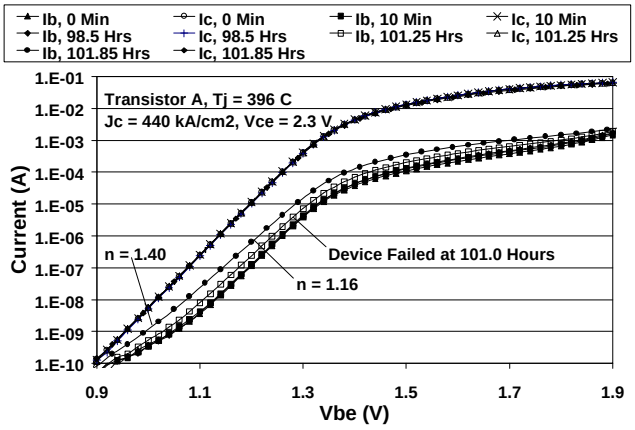

Fig. 1. Gummel plots of Transistor A measured at different stages of WLR stress. The stress current density was 440 kA/cm^2.

When the device was stressed further, the current gain continued to drop rapidly. The gummel plots were measured again after 101.85 hours of stress and also plotted in Fig. 1. The degradation in current gain was caused by a predominant increase of "1kT" current component in base current. The increase in base current in the low current region remained low, and the increase in base current in the high current region was obvious. Similar degradation behavior was observed in transistors biased at other stress conditions given in Table I, namely an increase in "1kT" base current leading to a sudden decrease in current gain. The changes in maximum current gain over stress time for all transistors are plotted in Fig. 2.

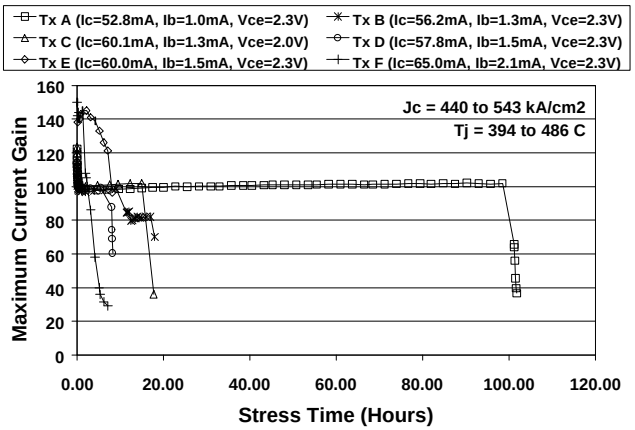

Fig. 2. Changes in peak room-temperature gain over stress time for the transistors listed in Table I.

We have monitored the ohmic contacts of the transistors under test. No degradation in any contact resistance was observed. The I_C versus Vbe curves stayed the same before and after test, indicating the property of the emitter junction was not affected. Fig. 3 compares the reverse gummel plots of Transistor A before and after stress. No significant change in the base-collector junction was observed. The current gain degradation observed here mainly comes from the base, and is analyzed in the next two sections.

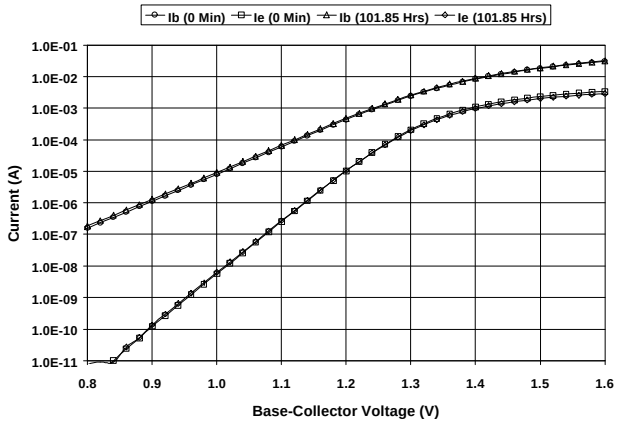

Fig. 3. Reverse Gummel plots of Transistor A before and after WLR stress. The stress current density was 440 kA/cm^2.

COMPARISON TO TRADITIONAL LOW CURRENT STRESS RESULTS

We also conducted traditional low current reliability test on 2 × 12 μm^2 InGaP HBTs at elevated temperatures in oven but with much lower current densities in comparison with those used in the WLR tests described above. A current density in the range of 50 to 75 kA/cm^2, and a junction temperature between 315 and 330 °C were used. The transistors were pretty reliable and lasted for 6000 hours before our failure criterion was met.

Fig. 4 shows different stages of traditional reliability tests done on a transistor stressed at 75 kA/cm^2 current density. The estimated junction temperature was 330 °C. The gain degradation behavior was similar to that observed in WLR tests, namely a long period of stable or small gradual degradation in current gain followed by rapid degradation caused by an increase in base current. However, the way that the base current increase was different from that shown in Transistor A under WLR stress at ultra high currents. As shown in Fig. 4, the failure criterion was first met after 6110 hours of stress. At this stage, the failure was triggered by a predominant "1kT" current component increase in base current. The increase in base current in the low current region remained low, and the increase in base current in the high current region in which the role of series resistance is important was evident. Upon stressing the transistor further for another 163 hours, the increase in the "2kT" current

component started to show up more, as reflected by the change to a higher ideality factor in the base current.

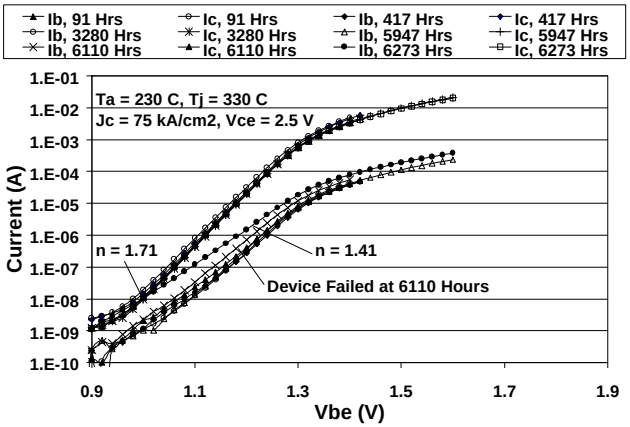

Fig. 4. Gummel plots of a 2 × 12 μm^2 InGaP HBT measured at different stages of traditional low current stress test in oven. The stress current density was 75 kA/cm^2.

Fig. 5 shows different stages of traditional reliability test done on another transistor stressed at an even lower current density of 50 kA/cm^2. In this case, the stress current density was only slightly above the critical density for the onset of Kirk effect. The estimated junction temperature was 315 °C. The current gain degradation behavior over time remained similar to those appeared in all WLR tested HBTs and in the transistor stressed at 75 kA/cm^2. The device did not degrade much after 6086 hours of stress, but failed suddenly upon further stressing for another 163 hours. The failed was caused by a predominant "2kT" base current component increase, as evidenced in the high ideality factor in the base current.

ROLE OF NEUTRAL BASE RECOMBINATION UNDER HIGH CURRENT STRESS

To understand how the current density affects the base current in transistor under high current stress, one can look into the five basic current components comprising the base current:

$$I_B = I_{NBR} + I_{SCR} + I_{TR} + I_{SR} + I_{pE} \qquad (1)$$

where I_{NBR} is the recombination current in the quasi-neutral base, I_{SCR} is the recombination current in the base-emitter space charge region, I_{TR} is the tunneling-recombination through mid-gap traps in the base near the base-emitter heterojunction [3], I_{SR} is the surface recombination at the emitter surface and base-emitter junction periphery, and I_{pE} is the injected hole current from the base into the emitter. Among them, I_{NBR} and I_{pE} carry "1kT" temperature dependence, I_{SCR} has a "2kT" behavior, I_{TR} has an ideality factor greater than 2 [3], and I_{SR} has its ideality factor decreasing from 2 to 1 as I_C increases [4].

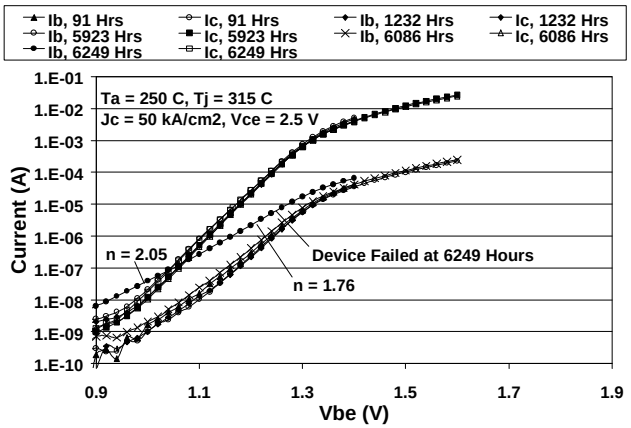

Fig. 5. Gummel plots of a 2 × 12 μm^2 InGaP HBT measured at different stages of traditional low current stress test in oven. The stress current density was 50 kA/cm^2.

In InGaP HBTs, the valence band discontinuity is large at the base-emitter heterojunction, and I_{pE} is therefore small even under large forward bias because of the large hole barrier. With the use of low surface recombination velocity InGaP emitter layer and a properly designed emitter ledge, I_{SR} is also small. It leaves only three dominant base current components in the base current equation: I_{NBR}, I_{SCR} and I_{TR}. Since I_{SCR} and I_{TR} are proportional to exp(qV_{BE}/nkT) with n 2, and I_{NBR} is proportional to exp(qV_{BE}/kT), I_{SCR} and I_{TR} are most significant when the current levels are low. At very high current levels at which base pushout is significant, I_{NBR} could dominate given its dependency on I_C and the widened base width, X_B:

$$I_{NBR} \approx \frac{qX_B A_E n_i^2}{2t_n N_B} \exp\left(\frac{qV_{BE}}{kT}\right) \approx \frac{I_C X_B^2}{2t_n D_{nB}} \qquad (2)$$

Eq. (2) is over-simplified in the sense that the minority electron recombination lifetime t_n is not the same between the base and the base pushout region, nor is the electron diffusion coefficient, D_{nB}. Qualitatively speaking, t_n is much smaller in the base than in the base pushout region because of the high trap density associated with the high impurity concentration and significant Auger recombination in the former. Though X_B and I_C are large, it is expected that the recombination rate remain low in the base pushout region when compared to that in the quasi-neutral base even under extreme base pushout condition.

It has been reported that the minority carrier lifetime in GaAs HBTs with base doping around 4 × 10^{19} cm^{-3} was limited by recombination at trap sites in the quasi-neutral base [5]. Hence, it is reasonable to assume that recombination-enhanced defect reaction (REDR) that happens in the base near the base-emitter heterojunction [3] could also happen deeper in the base under high level injection, leading to an overall decrease in minority electron lifetime, t_n, over stress time. The energy (1.4 eV) released due to band-to-band electron-hole recombination could

generate a number of defects deeper in the base, and not only the mid-gap traps near the base-emitter heterojunction that contribute to tunneling recombination of high ideality factor at low currents as suggested in Ref. [3]. Thus, we believe that it is this increase in trap density deep in the base that led to the observed predominant increase in "1*kT*" base current component in the HBTs stressed under the extreme current levels in the WLR tests. The Gummel plots shown in Fig. 4 indicated that a mixed mode of failures caused by an increase in both "1*kT*" and "2*kT*" base current components when the stress current was raised from 50 to 75 kA/cm^2, presumably due to an increase in trap density in both the base-emitter SCR and the quasi-neutral base.

The above hypothesis appeared to be supported by the results given in Table I. We plotted the lifetimes of these transistors against the applied base currents in Fig. 6. Although the findings were preliminary, the lifetimes appeared to be related to the base currents used in biasing the transistors at very high stress currents. Devices stressed with lower base currents showed longer lifetimes than devices biased at high base currents. For example, Transistors B & C, which were biased at the same I_B of 1.3 mA, showed about the same lifetimes despite the fact that they ran at different current densities and junction temperatures, and similarly for Transistors D and E which were biased at the same I_B of 1.5 mA. The electron-hole recombination creates crystalline defects deep in the base that ultimately leads to degradation in current gain.

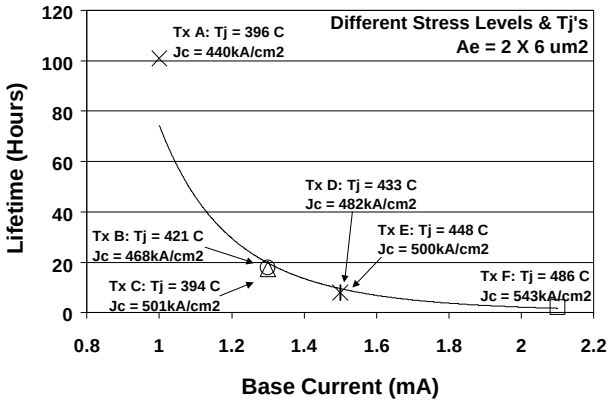

Fig. 6. Lifetimes of InGaP HBTs plotted as a function of applied base currents.

WLR TESTING FOR HBT RELIABILTY

The above analysis suggests that the location of generated defects at current levels much beyond that required for base pushout effect to occur could be different from that at low current levels. WLR testing at high currents cannot therefore replace traditional reliability testing at low currents for the prediction of HBT lifetime and extraction of activation energy under the normal "use" conditions.

CONCLUSIONS

We have performed wafer level reliability tests on InGaP HBTs using current densities much beyond that required for base pushout. The current gain degradation behavior appeared to be similar to that in traditional reliability test with the presence of a relatively long stable or slow gradual degradation region, followed by a sudden rapid degradation phase. The failure mechanism was, however, triggered by a predominant increase in "1*kT*" base current component, in contrast to a "2*kT*" base current increase at low current densities. The base current also seemed to play a very important role in the ultimate lifetime under very high current density condition. We hypothesize that the degradation of current gain was caused by generation of defects deep in the base due to increased neutral base recombination under severe base pushout. However, these defects are generated in locations different from those generated at low currents. WLR tests at currents much beyond base pushout should not be used to predict HBT lifetime and extract activation energy under the normal "use" conditions. Our devices were very reliable and did not show signs of degradation in reasonable time if less stressful condition was used in WLR testing.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
WLR: Wafer-Level Reliability
SCR: Space-Charge Region
REDR: Recombination-Enhanced Defect Reaction
BJT: Bipolar Junction Transistor