

Failure analysis of electrostatic discharge in InGaAs/AlGaAs PHEMTs

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Abstract

The performance against ESD stress of InGaAs/AlGaAs PHEMTs with Ti/Pt/Au and Ti/Al/Ti gate metallizations was studied. The Ti/Al/Ti gate PHEMT had a higher threshold voltage under the ESD stress than that of the Ti/Pt/Au gate PHEMT. Based on the failure analysis, it was indicated that the tapered Au that was formed on the semiconductor surface by Au movement from the Ti/Pt/Au gate electrode during the device manufacturing process, tended to laterally electromigrate due to the assistance of the electric field. On the other hand, Ti/Al/Ti metallization was more stable. The ESD failure of the Ti/Al/Ti-gate PHEMT occurred at the mesa-step edge, the region with concentrated electric field, under the higher ESD stress.

Introduction

GaAs devices are widely used in microwave communication systems. The increase of the device operating frequency was achieved by a rapid decrease of device geometry. These trends enhance the more sensitivity against the electrostatic discharge (ESD) [1,2]. Because no ESD-protection circuits are yet available in a small package, the development of the manufacturing process of the discrete PHEMTs is an important objective.

In this paper, we studied the leakage current behaviors of the gate diodes in PHEMTs under ESD stress and the physical analysis for the failure chips. The ESD sensitivities and failure mechanism were different between the two types of gate metallizations, Ti/Pt/Au and Ti/Al/Ti.

Experimental

The cross-sectional view of the InGaAs/AlGaAs PHEMT used in this study is shown in Figure 1. The gate length was 0.5 μ m and the total gate width was

432 μ m. Two different types of metallizations, Ti(20nm)/Pt(30nm)/Au(450nm) and Ti(20nm)/Al(500nm)/Ti(80 nm), were fabricated as the gate electrodes. The ohmic contacts with a thickness of 200nm comprised Ni/AuGe alloys. The devices were isolated by using wet chemical mesa etching and passivated with Si₃N₄ and SiO₂ layers.

ESD pulse voltages were applied to the gate electrodes in reverse direction against the source electrodes as shown in Figure 1. The experiments with ESD stress were performed according to the Human Body Model following the standard MIL-883 [4]. The voltages were increased in steps of -20V starting with -40V, until the gate leakage currents I_{gss} were beyond 40 μ A at -2V.

The ESD failure positions were detected by using Emission Microscopy (EMS) and Optical Beam Induced Resistance Change (OBIRCH) method [5]. The OBIRCH method has been practically used to detect any problems in the current pass, when it is difficult to observe the emission by EMS.

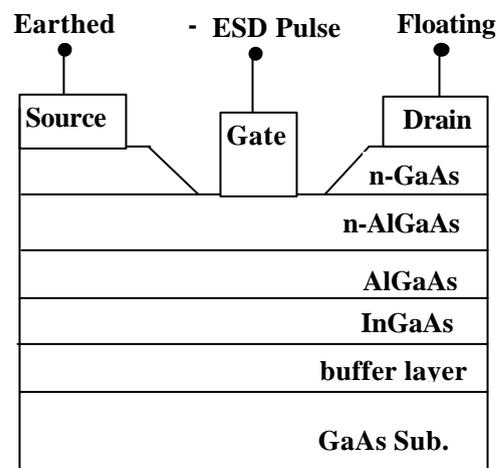


Figure 1. InGaAs/AlGaAs PHEMT cross-sectional view.

Results and Discussions

(1) Leakage current behaviors after the ESD stress

Figure 2 shows the typical I_{gss} values versus the ESD applied voltages of PHEMT with Ti/Pt/Au gate (Au-gate PHEMT) and that with Ti/Al/Ti (Al-gate PHEMT).

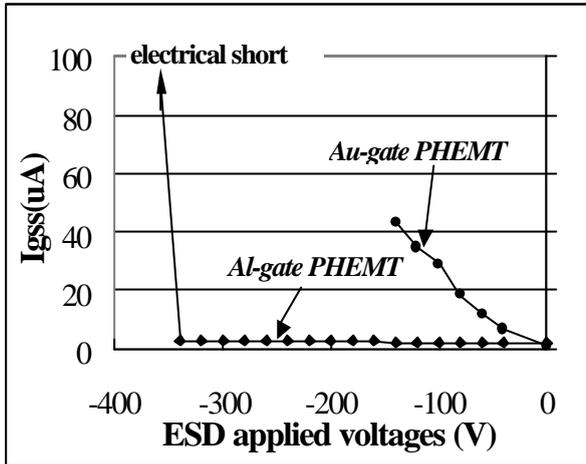


Figure 2. Typical I_{gss} versus ESD applied voltages of Au-gate and Al-gate PHEMTs

The Au-gate PHEMT had a lower threshold voltage against the ESD stress than that of the Al-gate PHEMT. The I_{gss} behaviors of the above two PHEMTs were different, as follows. The I_{gss} of Al-gate PHEMT increased little with the ESD voltages and suddenly the source, the drain and the gate were electrically shorted at the threshold voltage.

On the other hand, the I_{gss} of the Au-gate PHEMT increased gradually with the ESD applied voltage. The I_{gso} (the drain was opened) showed a behavior similar to that of the I_{gss} , and the I_{gdo} (the source was opened) increased slightly as shown in Figure 3. In the case that the ESD pulse voltages were applied between the gate electrodes and the drain electrodes, the reverse behaviors were observed between the I_{gdo} and the I_{gso} ; the increase of I_{gss} was mainly for the I_{gdo} and the I_{gso} showed little increase.

The above results indicated that the failure occurred in the diode region between the gate and the ohmic electrode where the ESD voltage was applied and did not occur at the Schottky contact.

The I_{gso} and I_{gdo} in Al-gate PHEMT both showed behaviors similar to those of the I_{gss} , independent of

the applied voltage direction to the drain or the source electrode.

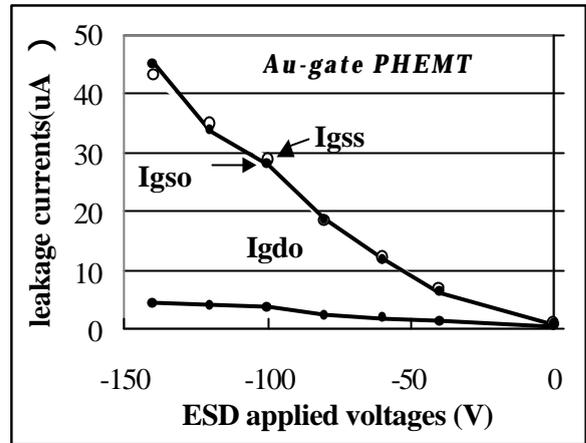


Figure 3. Typical I_{gss} , I_{gso} and I_{gdo} versus ESD applied voltage of Au-gate PHEMT.

(2) Failure position analysis

Figure 4 shows the EMS image from the failed chip of the Au-gate PHEMT. The I_{gss} of the failed chip was about 50uA at -2V, and the EMS image was obtained under the condition that the I_{gso} was 87uA at -29V.

The emissions indicating the damaged regions were observed around the gate electrode lines. All the failed Au-gate PHEMT chips had similar emission patterns between the gate and the source electrode. These patterns varied depending on the failure portions.

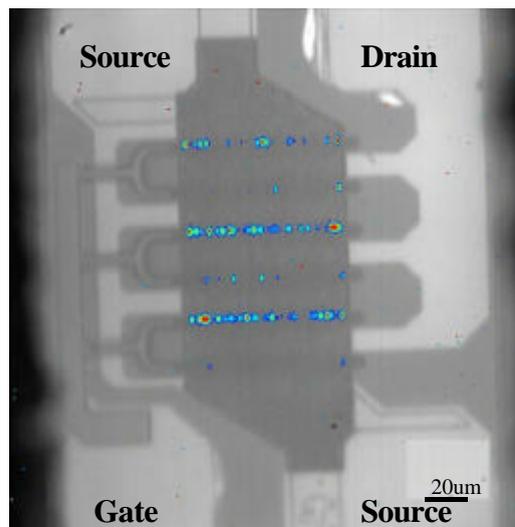


Figure 4. EMS image from the failed chip of the Au-gate PHEMT.

In the case of the Al-gate PHEMT, no EMS emission was detected in all the failed chips. Because, as indicated in Figure 2, the electrical failure mode was a short, the emission obtained from the failed chip was feeble radiation. Therefore, we tried to apply the OBIRCH method to detect the short positions. The OBIRCH was performed for the failed chip under I_{gso} 45uA at -0.15V. The signal, shown in Figure 5, was detected at the cross position of the gate electrode line and the mesa-step line used for the device separation. No signal was observed along the gate electrodes unlike in the case of the EMS image from the failed Au-gate HEMT chips.

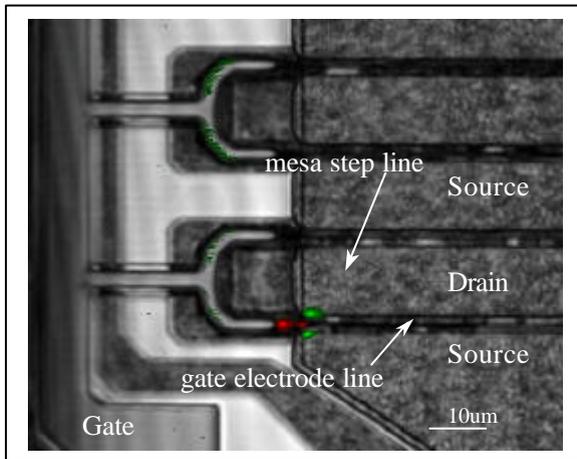


Figure 5. OBIRCH image from the failed chip of the Al-gate PHEMT.

(3) TEM observations

Figures 6 and 7 show the cross-sectional TEM images around the gate metallization in the Au-gate PHEMT and Al-gate PHEMT, respectively. Figure 6 confirms that the Au metal in the gate electrode contacts onto the epitaxial n-AlGaAs layer, forming the tapered edge. It was surmised that the Au metal migrates thermally toward the semiconductor surface during the device manufacturing, in greater and lesser degrees.

On the other hand, no migration from the gate metallization occurred even in the failed chips of Al-gate PHEMT shown in Figure 7. This observation was consistent with the OBIRCH result shown in Figure 5 that no signals were detected around the gate electrodes.

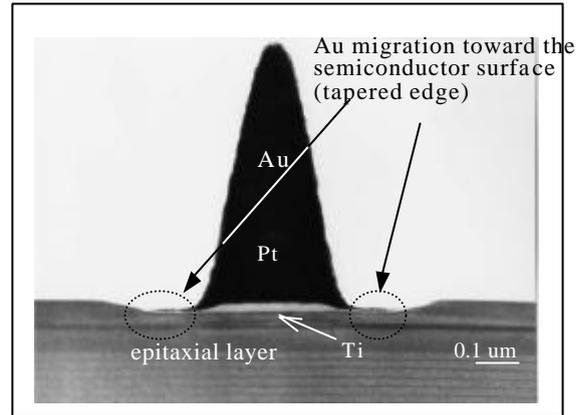


Figure 6. Cross-sectional TEM image of the Au-gate PHEMT around the gate electrode.

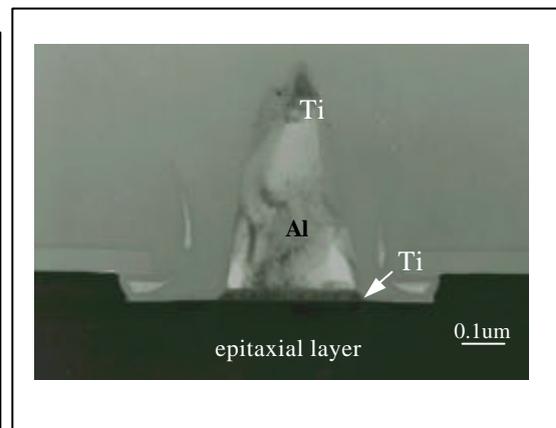


Figure 7. Cross-sectional TEM image around the gate electrode in the failed Al-gate PHEMT chip.

The cross-sectional view image along the gate line direction around the OBIRCH signal position shown in Figure 5 was observed by TEM (Figure 8). The semiconductor crystal defects extended from the edge of the mesa-step under the gate metallization. Consequently, a lot of crucial crystal defects were found to be generated around the active layer and the interface between the epitaxial layer and the substrate.

(4) Failure mechanism

On the basis of the above experimental results, the failure mechanism in the two different gate metallizations, Ti/Pt/Au and Ti/Al/Ti, is described as follows.

Au metal in the Ti/Pt/Au electrode moves toward the epitaxial semiconductor surface even during the device manufacturing process. The initiation of electric

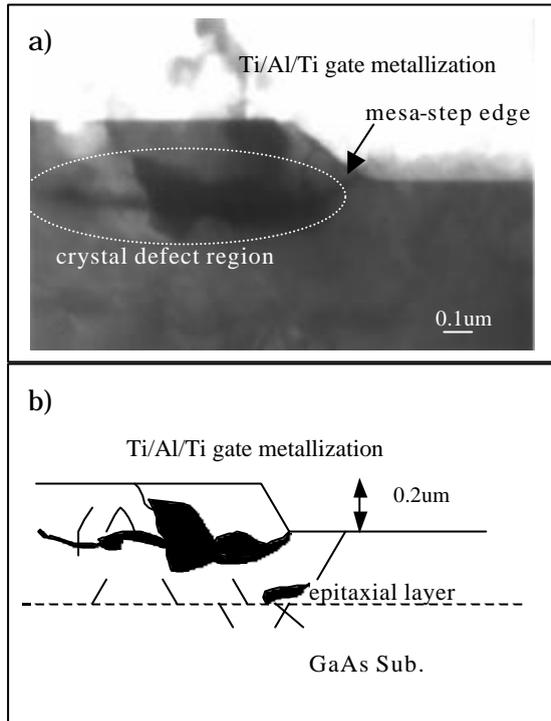


Figure 8. Cross-sectional, along the gate electrode direction, TEM image of the failed Al-gate PHEMT chip at the OBIRCH signal position shown in Figure 5.

a) TEM photograph, b) the illustration.

field assists the metal tapered on the semiconductor surface to laterally electromigrate between the two neighboring electrodes, the gate and the source. With the enhancement of the migration by the ESD stress, the surface leakage current is gradually increased and finally exceeds a maximum permissible level of the device operation. Because Au metal seems to possess various kinds of tapered figures and angles, the degradation positions might be dispersed around the gate electrodes.

In Ti/Al/Ti metallization, Al metal is more stable during the manufacturing process and is less prone to electromigration by ESD stress, than is Au metal. Therefore, the PHEMT with Ti/Al/Ti gate exhibits a better performance against ESD. Nevertheless, when a

higher ESD stress is applied, the epitaxial semiconductor degradation or defects occur from the mesa edge under the gate electrode, where the electric field is concentrated. The metallization might diffuse into the epitaxial layer through these defects, finally leading to an electrical short.

Conclusions

In conclusion, electrical and physical failure modes of the ESD stress were different in two kinds of PHEMTs with Ti/Pt/Au gate and Ti/Al/Ti gate. The devices with the electrodes containing Au metal were weak against the ESD stress because of the Au electromigration from the tapered edge that was formed by Au metal movement during the device manufacturing process. The devices with Au-less electrode such as Ti/Al/Ti exhibited a better performance because of no the electromigration by the ESD stress. In this case, the generation of defects at the gate mesa edge caused a sudden failure under the higher ESD stress. In either PHEMT case, the basic failure origins were attributed to the regions with high electric field concentration.

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