A Power Law Model for Assessment of Hot Electron Reliability in GaAs MESFETs and AlGaAs/InGaAs pHEMTs

Val Kaper*, Peter Ersland

M/A-COM Engineering & Technology Group
100 Chelmsford Street; Lowell, MA 01851
(978) 656-2817; erslandp@tycoelectronics.com

Abstract

Hot electron reliability experiments were conducted on four GaAs FET processes. Observed device degradation was similar to the results reported by other authors (e.g. decrease of the open channel current, and a rightward shift and compression of the transconductance curve). While the degradation modes were the same for all four processes, the degradation rates were not. These results have led us to propose that the existing figure of merit model [1] should be extended to a power law model, thereby incorporating the dependence of device degradation rate on the reverse gate-drain current density. The power law model coefficients along with the breakdown voltage provide complete information about susceptibility of a particular process to the hot electron induced degradation, and also indicate reliability limitations on what type of dynamic load line and input power level can be safely used.

INTRODUCTION

The problem of hot electron induced (HEI) degradation in GaAs-based FET devices arises when a device is driven into breakdown by a combination of the DC bias and input power drive. In this state, a transistor is subjected to high electric fields that provide some number of electrons with energy sufficient to escape from the channel and potentially become trapped in the passivation layer – semiconductor interface. This trapped charge results in a portion of the channel remaining unmodulated by applied gate bias, leading to a reduction of the open-channel current (I_{max}) and maximum power density. These changes in DC characteristics adversely affect device performance in amplifier applications.

Several groups have made significant contributions to our understanding of the hot electron and RF overdrive effects in compound semiconductor FETs over the past several years [1]-[10]. However, very few attempts have been made to quantify device reliability under these extreme conditions, or to extrapolate these results to typical use conditions. Leoni et al [1] and Tkachenko et al [8] used a figure of merit to compare hot electron reliability of various MESFET and pHEMT processes. Physically, this figure of merit corresponds to the negative charge density that has to be forced through the Schottky gate for a FET to parametrically fail. It is calculated as the product of gate current density and the time required for the device open channel current (I_{max}) to decrease by 10%, normalized to A*hours/m. This model, however, does not match our experimental observation, that different devices exhibit different rates of change in lifetime at different reverse gate current levels.

For reference, the common way to measure hot electron reliability in Si MOSFETs is to use an experimentally determined dependence [11]

$$TTF \propto \exp\left(\frac{1}{V_{DS}}\right),$$

where TTF is an appropriately defined time to failure; and V_{DS} is drain-source voltage, at some constant gate voltage corresponding to the maximum substrate current [12].

For MOSFET devices there is a strong relationship between V_{DS} and the maximum electric field in the device channel ($E_{max} \propto (V_{DS} - V_{knee})$); therefore V_{DS} is a reliable indicator of the probability for hot electron degradation to occur. In contrast, most compound semiconductor FET devices use a recessed gate configuration, which is susceptible to a certain degree of variation in the gate recess depth. This variation is a cause for a weaker correlation between maximum electric field in the device channel and V_{DS}. As a result, gate current is seen as a better predictor of HEI degradation in compound semiconductor FETs than V_{DS} or V_{DG}.

In this paper, we propose a new empirical model, which can be used to accurately compare hot electron reliability of compound semiconductor FETs from different processes. This model is a more general case of the figure of merit model used in references [1], [8].

* Val Kaper is now with Cornell University; Ithaca, NY

EXPERIMENTAL

Hot electron reliability was investigated on four different compound semiconductor FET processes. These processes are:

1) 0.5 µm switch/power pHEMT;
2) 0.18 µm mm-wave low noise pHEMT;
3) 0.5 µm recessed gate ion-implanted MESFET; and
4) 0.5 µm self-aligned gate ion-implanted MESFET.

To ensure a fair comparison, the same device layout, a two-finger 600 µm wide FET, was manufactured on all four processes; the only difference being the gate position in relation to drain and source ohmic contacts. DC characteristics (transfer, transconductance and I_{DSS} curves) of typical devices manufactured on these four processes are presented in Figures 1-3.

Prior to and periodically during the stress, all devices were thoroughly characterized using an HP4142 Source-Monitor unit. The measured device parameters included: transfer and transconductance curves at V_{DS} = 1.5V, an I_{DSS} curve, open-channel current I_{max} at V_{DS} = 1.5V and I_G = 1mA/mm, two-terminal gate-source breakdown voltage BV_{GS} at I_G = -1mA/mm, and Schottky gate-source diode turn-on voltage at I_G = 1mA/mm.

During the stress, device degradation was accelerated by forcing reverse gate currents ranging from –0.2 mA/mm to –70 mA/mm. These four processes each exhibit different susceptibility to catastrophic failure during reverse gate current stress. Since the purpose of these experiments is to accelerate parametric degradation without causing catastrophic failure, the range of gate currents was different for each process. As there was no easy way to float the source during the stress, the reverse gate current forced by HP4142 was divided between grounded source and drain terminals approximately according to the ratio l_{GD}/l_{GS}, where l_{GD} and l_{GS} are gate-drain and gate-source spacing, respectively. The drain current measurement in this test configuration represents the value of the reverse gate-drain current, which was used in the subsequent reliability model development.

The change in I_{max} as a function of stress time for selected devices from all four processes is depicted in Figure 4. With exception of the self-aligned MESFET, all devices exhibit a nearly constant rate of degradation over time. RF overdrive experiments on the 0.5 µm pHEMT process [16] have shown that normal gate and elevated drain bias, in conjunction with high compression RF input drive, results in degradation rates for P_{out}, I_{max} and I_{DSS} similar to those observed under DC stress conditions.

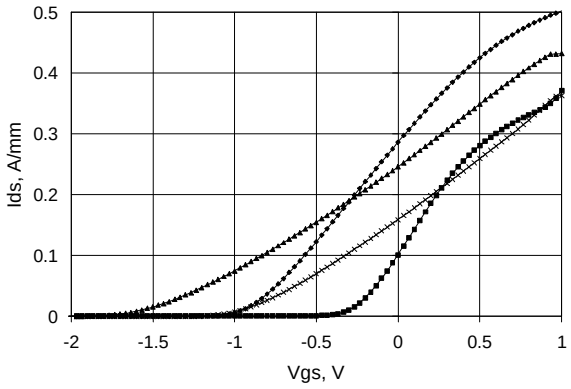

Figure 1 Transfer curves (at V_{DS}=1.5V) of devices from four processes: 0.5 µm pHEMT ( ), 0.18 µm pHEMT ( ), 0.5 µm recessed gate MESFET ( ), 0.5 µm self-aligned gate MESFET (+)

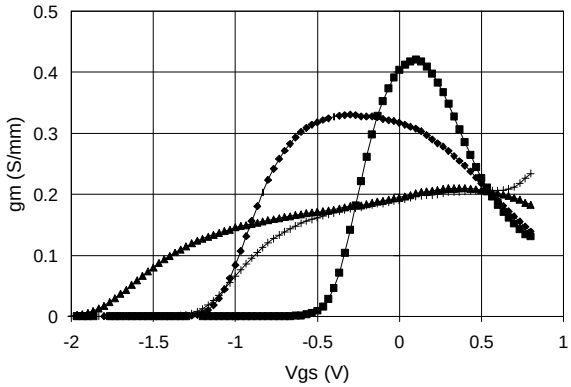

Figure 2 Transconductance curves (at V_{DS}=1.5V) of devices from four processes: 0.5 µm pHEMT ( ), 0.18 µm pHEMT ( ), 0.5 µm recessed gate MESFET ( ), 0.5 µm self-aligned gate MESFET (+)

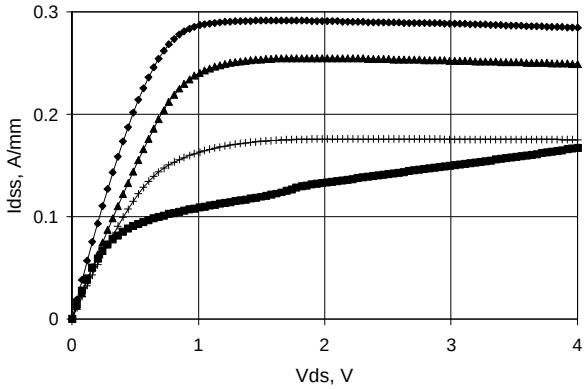

Figure 3 I_{DSS} curves (at V_{DS}=1.5V) of devices from four processes: 0.5 µm pHEMT ( ), 0.18 µm pHEMT ( ), 0.5 µm recessed gate MESFET ( ), 0.5 µm self-aligned gate MESFET (+)

Figure 5 shows time to failure (10% decrease in I_{max}) as a function of the reverse gate-drain current density for three stressed processes: 0.5 µm pHEMT, 0.18 µm pHEMT and 0.5 µm recessed gate MESFET. Data for the 0.5 µm self-aligned MESFET process is absent from this chart due to the fact that on all tested devices from this process the degradation saturated after reaching approximately 6%.

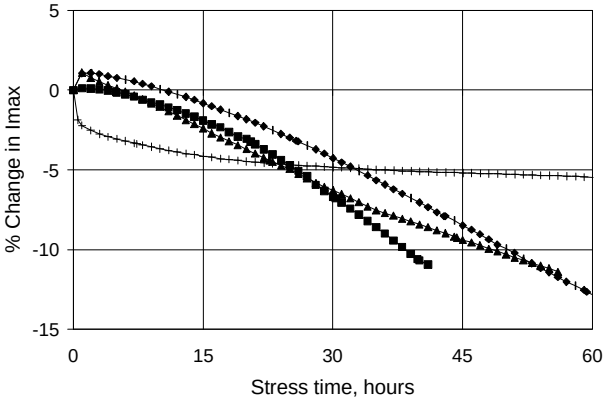

Figure 4 I_{max} degradation vs. time under hot electron stress for devices from four processes: 0.5 µm pHEMT ( ), 0.18 µm pHEMT ( ), 0.5 µm recessed gate MESFET ( ), 0.5 µm self-aligned gate MESFET (+)

POWER LAW MODEL

According to the figure of merit model, used in references [1] and [8], time to failure, defined as 10% decrease in the open-channel current, is a single variable (FM) function and can be calculated as

$$TTF = FM * \left(\frac{l_{GD}}{l_{DS}} \right) * \left(\frac{|I_G|}{W} \right)^{-b}$$

where TTF is time to failure in hours (10% decrease in I_{max});
FM is an experimentally determined process dependent variable (in A*hours/m);
l_{DS}, l_{GD} are drain-source and gate-drain distances respectively;
I_G is total reverse gate current in A;
W is gate width in m; and
b=1 is a constant.

Our experimental data, presented in Figure 4, suggests that b is not a constant, but rather a process dependent variable. Given these results, the figure of merit model should be extended to a power law model in order to accurately compare the hot electron reliability of different processes at various gate current stress levels. Device

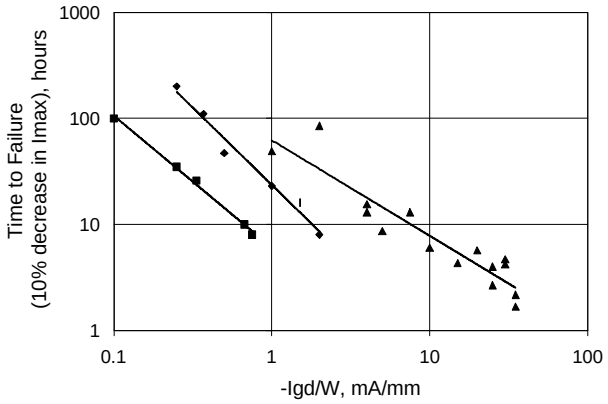

Figure 5 Device lifetime as a function of reverse gate-drain current density: 0.5 µm pHEMT ( ), 0.18 µm pHEMT ( ), 0.5 µm recessed gate MESFET ( )

lifetime in the power law model is a function of two variables and can be expressed as follows:

$$TTF = TTF_{J_0} * \left(\frac{|I_{GD}|/W}{|J_0|} \right)^{-b},$$

where TTF_{J_0} is time to failure in hours at $J_{GD} = J_0 = -1$ mA/mm; and
$J_0 = -1$mA/mm is a normalization factor, necessary to keep the dimensions consistent.

Values of TTF_{Jo} and b, along with open-channel current and two-terminal breakdown voltages for the four processes we have tested, are shown in Table 1. In order to include TTF_{Jo} and b parameters for the 0.5 µm self-aligned MESFET process, we have used time corresponding to 5% decrease in I_{max} to calculate the factor b, assuming that b does not depend on the choice of the failure criteria as long as it lies in the linear degradation region. TTF_{Jo} for this process was obtained by doubling the mantissa of the 5% power law fit.

TABLE 1
Open channel current (I_{max}), two-terminal breakdown voltage (BV_{GS}), and power law model parameters for four different processes

Process	I_{max} mA/mm	BV_{GS} V	TTF_{Jo} hours	b
0.5 µm pHEMT	500	-18	21.9	1.55
0.18 µm pHEMT	230	-6	6.0	1.25
0.5 µm MESFET (recessed)	400	-14	43.8	0.87
0.5 µm MESFET (self-aligned)	330	-11	917.1	0.85

DISCUSSION

Qualitatively, power law parameters TTF_{Jo} and b are analogous to mean time to failure (*MTTF)* and activation energy (E_a) in the Arrhenius model, commonly used for measuring device reliability due to temperature activated degradation mechanisms, such as gate sinking [13], ohmic contact degradation [14], "hydrogen poisoning" [15] et cetera. Similar to E_a, assuming the same TTF_{Jo} for two different devices, the transistor with larger magnitude of b will have longer *TTF* at operating gate current levels. Since hot electron reliability of a FET ultimately depends on the peak electrical field in the channel of a device, b also indicates the degree of correlation between reverse gate-drain current density and peak electric field.

It is remarkable to note that both pHEMT processes have exponential factors b larger than 1, while b for both MESFET processes is less than 1. In agreement with this observation, experimental data presented by Tkachenko et al [8] can be used to extract b equal to 1.3 for 0.8 μm pHEMT and 0.68 for 0.8 μm epitaxial MESFET. Therefore, following statements can be made:

1) the hot electron reliability of pHEMT exhibit greater dependence on the reverse gate current density than for MESFET, meaning that *TTF* of a pHEMT is expected to increase more rapidly as operating gate current is reduced, and conversely to decrease more rapidly as I_G increases;
2) reverse gate-drain current density is a better measure of the peak electric field in pHEMT than in MESFET.

One important remark that needs to be made is that it would be erroneous to consider power law model coefficients alone as sufficient criteria to judge the hot electron reliability of a particular device. Since different devices require different bias conditions to obtain the same value of the gate current, one must also consider the device breakdown characteristics. For example, a device with low breakdown voltage would still be unsuitable for power applications even though it might exhibit acceptable reliability with respect to the power law model coefficients.

CONCLUSION

We present a new model, which allows us to accurately compare hot electron reliability for different MESFET and pHEMT processes, and potentially can be used in other compound semiconductor FET processes. The power law model coefficients, along with the breakdown voltage, provide complete information about susceptibility of a particular process to the hot electron induced degradation

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ACRONYMS

MESFET: Metal-Semiconductor Field Effect Transistor
pHEMT: pseudomorphic High Electron Mobility Transistor
HEI: Hot Electron Induced [Degradation]
MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor
TTF: Time to Failure