New method to monitor the frequency-dispersion in InGaAs/AlGaAs PHEMTs

Takayuki Izumi, Tomoyuki Ohshima, Masanori Tsunotani and Tamotsu Kimura

III-V Devices Department, Optical Components, Oki Electric Industry Co., Ltd.
550-1 Higashiasakawa, Hachioji, Tokyo 193-8550, Japan
Phone: +81-426-62-6669, Fax: +81-426-62-6616, E-mail: izumi173@oki.com

Abstract

The frequency-dispersion of PHEMTs with buried gate structures has been evaluated using the drain current transient measurement. We have observed a trap with a time constant of 9.0 μsec as an origin for the frequency-dispersion, which is closely correlated with the device structure. In order to quantitatively characterize the frequency-dispersion of the PHEMTs, we have introduced a new parameter of ΔVth, which can be defined as a difference of threshold voltages for the devices with and without the inner recess. Then, we demonstrate that the Vth is quite effective to evaluate the frequency dispersion and to predict the power degradation at high-frequency operation.

INTRODUCTION

The InGaAs/AlGaAs pseudomorphic HEMTs (PHEMTs) have demonstrated superior high-power performances in wide-range frequencies. One of the most important issues in PHEMTs is to suppress the frequency-dispersion of the device characteristic such as a gate-lag phenomenon, which could be related to the surface states in the ungated region beside the gate [1][2]. The frequency-dispersion causes power degradation of PHEMTs at high frequency, and might lead to a decrease in their performances for long-term operation. In order to evaluate the frequency-dispersion of the device, the pulsed I-V measurement has been used, in which the transient of the drain current following the pulsed gate bias can be observed. However, from a manufacturing point of view, a more simple method to use for in-process monitoring is desirable to check the device quality with respect to the frequency-dispersion. In this paper, we propose a new method to predict the frequency-dispersion of PHEMTs only by using a simple DC measurement.

EXPERIMENTAL

Figure 1 shows a cross-section of the double-recessed $In_{0.2}Ga_{0.8}As$ / $Al_{0.28}Ga_{0.72}As$ PHEMT with a buried gate structure used in this study, in which the inner recess region was completely covered by the T-shaped Au/Pt/Ti gate metal. Such a buried gate structure has been widely used for power PHEMTs or MESFETs to suppress a frequency-dispersion with high breakdown voltage [2][3]. The gate length defined by the inner recess width was 0.6 μm and the length for the top portion of the T-shaped gate was 1.0 μm. The outer recess widths were 0.25 μm and 0.65 μm for the source and the drain sides, respectively. The epitaxial layer structures were grown by MOCVD.

In order to systematically investigate a relationship between the device structure and the frequency-dispersion, the samples with different threshold voltages (Vth) and the 2DEG densities (Ns) were prepared by changing the Schottky and the doping layer thickness. The inner and the outer recess depths were also changed by controlling the wet-etching time for the undope GaAs layer. After the Au/Pt/Ti gate electrode was formed using electron-beam evaporation and lift-off processes, the SiN/SiO_2 passivation films were deposited on the device region by PECVD (Plasma Enhanced Chemical Vapor Deposition) and LPCVD (Low-Pressure Chemical Vapor Deposition), respectively.

The frequency-dispersion for the device was characterized using the test configuration in fig. 2. The gate width of the device was 10 μm. After a pulsed gate bias was applied, a transient for the drain current was measured using a digitizing oscilloscope through a 100 ohm load. The pulse width and period for the gate bias were set to 100 msec and

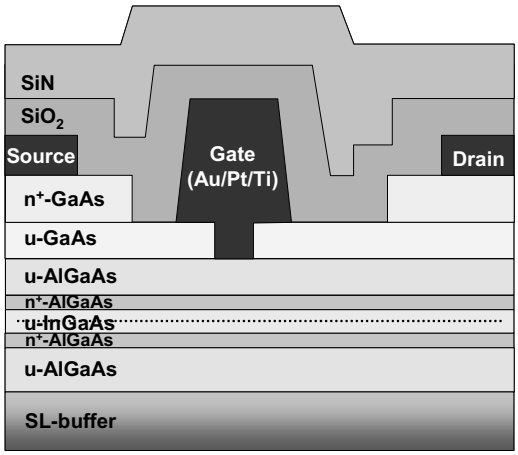

Fig.1 Cross-section of InGaAs/AlGaAs PHEMT with a buried gate structure.

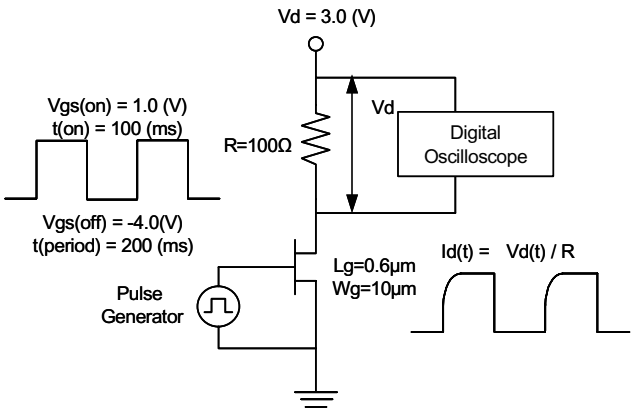

Fig.2 The electrical schematic diagram of the drain current transient.

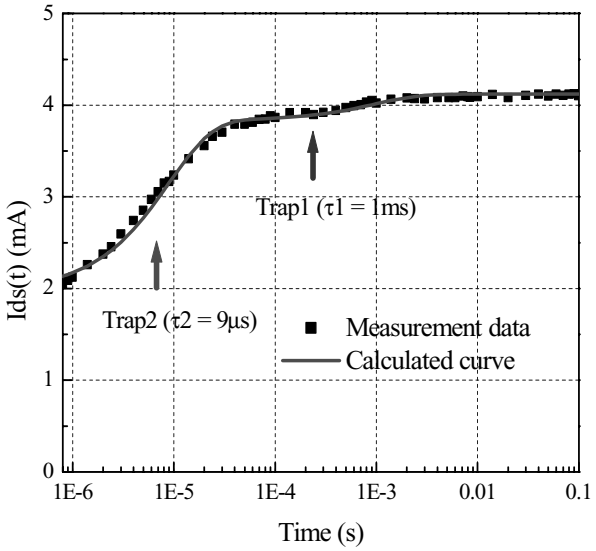

Fig.3 A typical drain current transient for the PHEMT.

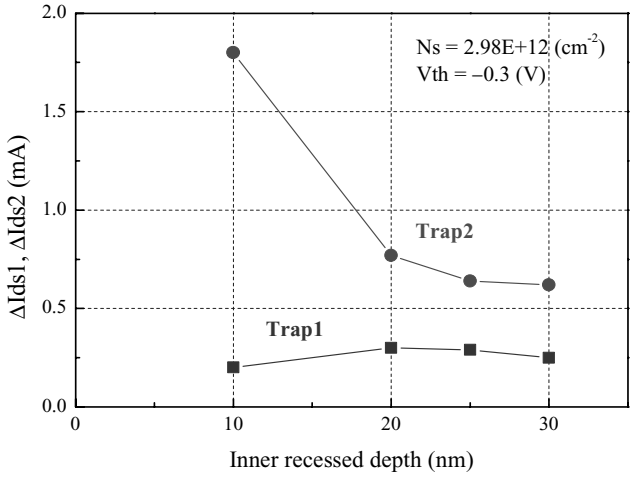

Fig.4 Dependence of ΔIds1 and ΔIds2 on the inner recessed depth.

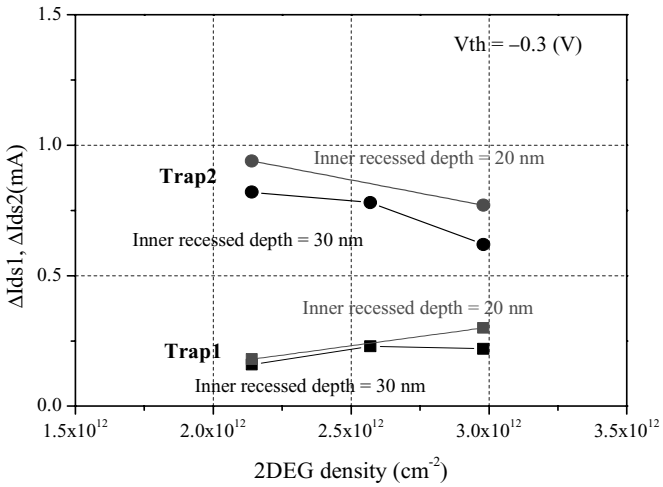

Fig.5 Dependence of ΔIds1 and ΔIds2 on the 2DEG density.

200 msec, respectively. The drain current reaches to its steady state during each pulse because a time constant for the transient is sufficiently short compared with the pulse duration. The threshold voltages of the samples were in the range from -0.3 V to -1.0 V, and the pulsed gate bias of -4 V / +1 V was applied at a constant drain voltage of +3 V.

MEASUREMENT OF DRAIN CURRENT TRANSIENT

The square points in fig. 3 show a typical drain current transient after the pulsed gate bias was applied. By fitting the measured data using exponential decay curves, the drain current transient can be expressed as,

$$Ids(t) = Ids0 - \Delta Ids1 \times exp(-t/\tau 1) - \Delta Ids2 \times exp(-t/\tau 2) \quad (1)$$

where Ids0 is the drain current at steady state and the other terms show the time-dependent current components due to the traps affecting the drain current transient. The τ and ΔIds would be correlated with the time constant and the density for the traps. The solid line in fig.3 illustrates the calculated curve by Eq.(1). In this case, we can fit the measured data by two kinds of traps named trap1 with τ1 of 1.0 msec and trap 2 with τ2 of 9.0 μsec, as shown in fig. 3. Figures 4 and 5 show the dependence of ΔIds1 and ΔIds2 on the inner recessed depth and the 2DEG density, respectively. The 2DEG density was varied by the doping layer thickness.

The threshold voltages for the devices in figs. 4 and 5 were controlled to be same for each inner recessed depth by changing the etching depth of the outer recess. As shown in figs. 4 and 5, the ΔIds2 decreased as increasing the inner recessed depth and the 2DEG density, while the ΔIds1 doesn't show any changing. This result clearly shows that the origin of the trap1 was in bulk region such as epi-layer / substrate interface and was not affected by the device structure. Moreover, the influence of ΔIds1 on the drain current transient was negligibly small for our devices compared with ΔIds2. Therefore, we focused on the trap2 to clarify the relationship between the device structure and the frequency-dispersion phenomenon.

As shown in figs 4 and 5, ΔIds2 can be suppressed by increasing the inner recessed depth and 2DEG density. This result means that a carrier concentration under the ungated surface region should be designed to be sufficiently large compared with that under the gate region to suppress the frequency-dispersion of the PHEMTs.

MONITORING METHOD OF FREQUENCY-DISPERSION

In order to quantitatively characterize the frequency-dispersion, we have introduced a new parameter of ΔVth, which was defined as a difference of threshold voltages between the PHEMTs with and without the inner recess. The ΔVth can be expressed as,

$$\Delta Vth = Vth1 - Vth2 \quad (2)$$

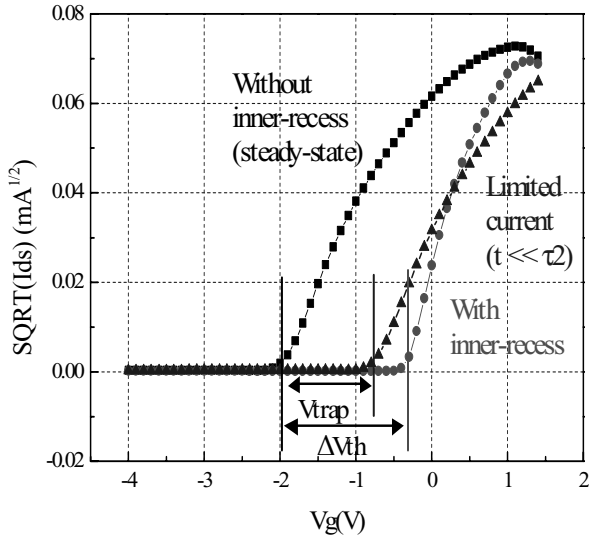

Fig.6 Concept of ΔVth for monitoring the drain current transient.

where Vth1 and Vth2 are threshold voltages for PHEMTs with and without the inner recess, respectively. The device without the inner recess can be easily fabricated on the same wafer just by skipping the inner recess-etching step and any additional process is not required. Therefore, the gate metal of the device without the inner recess was deposited on the un-doped GaAs layer. As increasing the ΔVth, the influence of the ungated surface on modulating the 2DEG in the channel could be expected to decrease, namely a difference of carrier concentrations between under the ungated surface and under the gate region becomes large.

Figure 6 simply illustrates the concept of ΔVth. The Ids-Vgs characteristics measured for the devices with and without the inner recess are shown in the figure by square and circle points, respectively. If we regard the ungated surface region besides the gate as a parasitic transistor connected with the intrinsic region in parallel, its Ids-Vgs characteristic can be simulated by the device without the inner recess. In a steady state, the intrinsic device, that is a PHEMT with the inner recess, limits the drain current because the current capacity for the parasitic transistor is sufficiently larger than that for the intrinsic one in all the gate biases. However, the threshold voltage for the parasitic transistor could shift to positive at just after the gate pulse is applied due to a slower response of a trapped charge in the surface states at SiO_2/GaAs interface. The triangle points in fig. 6 show the drain current for the parasitic transistor just after the gate pulse is applied ($t << \tau 2$). In this case, the extrinsic transistor collapses the maximum drain current for the intrinsic transistor. Therefore, the drain current gradually increases after the gate pulse is applied because the threshold voltage for the extrinsic transistor returns to its steady state by emitting carriers trapped in surface states with the time constant of τ2. The magnitude of the change in the threshold voltage for the extrinsic transistor (Vtrap) could be related to the surface state density. In order to suppress the frequency-dispersion of the drain current for the PHEMTs, the ΔVth should be sufficiently larger than Vtrap.

Figure 7 shows the dependence of ΔIds2 on ΔVth for various PHEMTs with different threshold voltages, 2DEG densities and inner recess depths. The ΔIds2 was normalized using Ids0 in the steady state. As shown in fig. 7, normalized ΔIds2 strongly depends on ΔVth, which suggests that the frequency-dispersion of PHEMTs can be well characterized by using the ΔVth. This method is also useful to predict the power degradation of PHEMTs in high frequency regions. Figure 8 shows the dependence of the output power (Pout) at 1 MHz on ΔVth. The output power was measured using the PHEMT of 140 μm width at the input power and the drain voltage of 5 dBm and 3 V, respectively. In spite of almost the same DC characteristics of those devices such as Idss and gm, the Pout strongly depends on ΔVth.

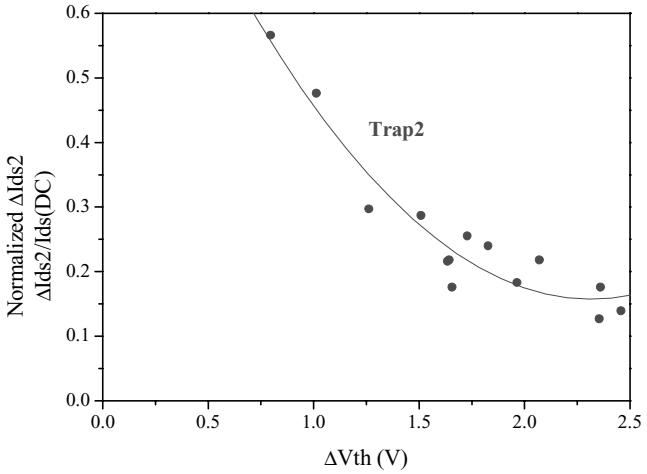

Fig.7 Dependence of normalized ΔIds2 on the ΔVth for various PHEMTs.

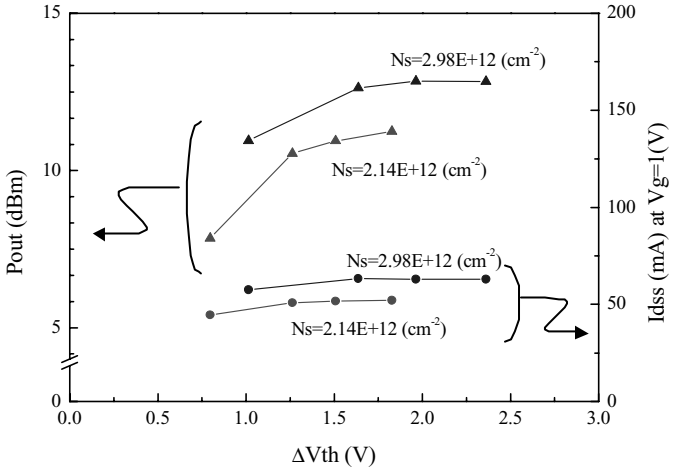

Fig.8 Dependence of the output power(Pout) at 1 MHz on ΔVth.

It can be concluded that the new parameter of ΔVth is very effective to characterize the frequency-dispersion of PHEMTs. Because ΔVth can be obtained by a simple DC measurement, it is also useful to control the high-frequency device performance in production line. Of course, it must be noted that the ΔVth should be optimized in terms of other device characteristics such as a breakdown voltage, which would also depend on ΔVth.

CONCLUSIONS

The frequency-dispersion of PHEMTs with buried-gate structures was evaluated using the drain current transient measurement. Then we found the trap2 with a time constant of 9.0 μsec as a main origin for the frequency-dispersion, which was closely correlated with the device structure such as inner recessed depth and 2DEG density. In order to quantitatively evaluate the frequency-dispersion for the devices with various structures, we introduced a new parameter of ΔVth, which was defined as a difference of threshold voltages between the PHEMTs with and without the inner recess. It was found that the ΔVth was quite effective to characterize the frequency-dispersion. In order to suppress the frequency-dispersion of the PHEMTs, the larger ΔVth was required. The ΔVth was also useful to predict the power compression of the device, because it could be obtained by a simple DC measurement.

REFERENCES

[1] Y. Kohno, H. Matsubayashi, M. Komaru, H. Takano, O. Ishihara and S. Mitsui: Tech. Dig. IEEE GaAs IC Symp., 1994, p.263
[2] James C. M. Hwang: Solid-State Electronics 43, 1999, p1325
[3] K. Matsunaga, N. Iwata and M. Kuzuhara: GaAs and Related Compounds, Karuizawa, 1992, p749