Dielectrically defined optical T-gate for high power GaAs pHEMTs

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Abstract

A dielectrically defined gate process has been developed that uses optical lithography to pattern near quarter micron T-gates. Record output power densities of 2.0 and 1.8 W/mm have been measured at 2 and 10 GHz, respectively. When applied to an X-band MMIC circuit, significantly higher power was measured. The new process offers improved performance and throughput compared to the standard e-beam defined T-gates. Initial results indicate that yield is better as well. These improvements are attributed to passivating the GaAs surface at an earlier step, resulting in fewer surface states and traps.

Introduction

A dielectrically defined near quarter micron T-gate process has been developed utilizing optical lithography. This process shows promise for increased yield and throughput compared to conventional quarter micron gate technology defined via electron beam lithography. By using this novel process improved RF performance, specifically higher output power density at 2 and 10 GHz, has been shown. The highest observed output power density (P1dB) at 10 GHz was 1.8 W/mm with 56% PAE and 13.8 dB gain. Additionally, enhancements to the FET DC output characteristics were demonstrated as well as improvements of the measured variances.

The developed process defines the trunk and cap of the T-gates in separate steps, which was first described by D Atwood [1] and also employed by Metze et al [2]. Those studies utilized e-beams to write the trunks and reported on the advantages of writing T-gates in two steps, including independent and improved control over the size and placement of the trunk and cap, faster write times and passivation at an earlier step for protection of the surface. The initial motivation for this new process was to improve wafer throughput by eliminating the time consuming e-beam patterning step. However, significant improvements in RF performance and yield have been found which are attributed to the preparation and passivation of the surface at an earlier step. Martinez et al [3] also showed significant RF performance improvement when they switched to a dielectrically defined process and eliminated a surface damaging etch-back step.

Process

The starting epitaxial material is the same used in the standard TriQuint Texas GaAs power pHEMT process. The layers include n+/n GaAs cap layers, and an InGaAs channel sandwiched between Si-pulse-doped AlGaAs layers. Ohmic contacts of Au/Ge/Ni/Au are made to the cap layers followed by implant isolation. A wide recess etch removes the cap layers.

In the new flow, processing is identical to the standard quarter micron flow through the ohmic, isolation and wide recess steps. Next, instead of patterning a T-gate profile with an electron beam, a thin PECVD layer of silicon nitride is deposited uniformly across the wafer. Nitride thickness is in the 1000-2000 A range, and the proper surface preparation prior to deposition is believed to be critical to RF performance. Gate stripes are then defined with a Canon I-line 5X stepper that can reliably pattern 0.33 μm in a single layer of photoresist. The patterned photoresist is over-coated with a shrink material, which is then baked and developed away. A small amount of the shrink material remains attached to the resist pattern, reducing the critical dimension (CD), Figure 1a. This

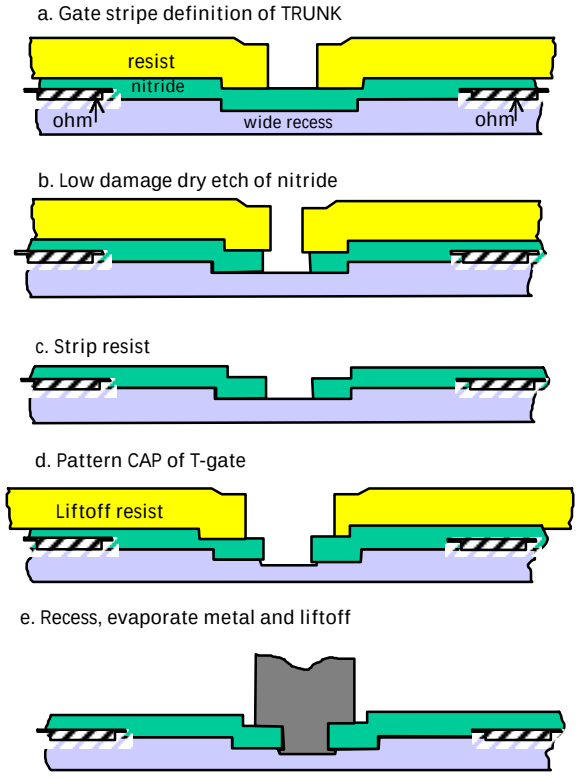

Figure 1. Diagram of process flow

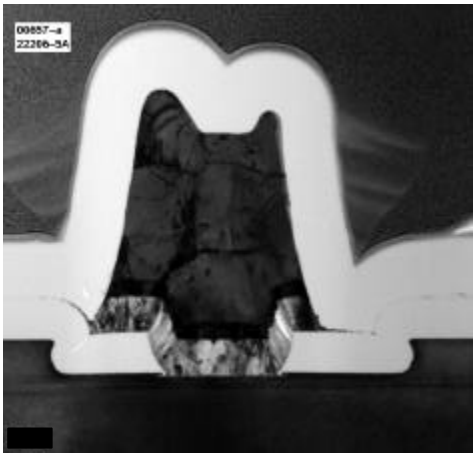

Figure 2. TEM showing finished optical T-gate defined in a layer of dielectric

process consistently shrinks the CD by approximately 0.1 μm, leaving a typical opening of 0.24 μm with a standard deviation of 6%.

The resist opening is then transferred into the nitride layer by dry etching, thereby forming the gate footprint, Figure 1b. In general, gate definition with dry etching techniques requires a low-damage etch process coupled with anisotropic profiles to maintain the necessary critical dimension (CD). The developed etch increases the CD by about 0.06 μm, and does not significantly damage the semiconductor. The photoresist is removed (Figure 1c) and the gate length is set by the nitride opening at the surface of the GaAs. The caps of the T-gates are then optically patterned using a standard resist with a liftoff profile (Figure 1d). At this point, the wafer is ready for standard gate recess which stops on an etch stop layer, metal deposition of Ti/Pt/Au and liftoff (Figure 1e). With careful control of the resist processing and dielectric etch, the optical process defines 0.30 μm gate-length T-gate structures (Figure 2). By using nitride as the recess mask instead of e-beam resist, there may be less undercut during gate recess. However, whatever undercut there is will result in a void of "vacuum passivated" GaAs [1] sealed by the trunk nitride and gate metal. This initially raised reliability concerns but has not been a problem (see Discussion).

A simpler single-step, optical lithographic process for the formation of delta gates has also been developed (using only steps shown in Figure 1a, 1b and 1e). Processing involves nitride deposition, photoresist definition and dry etching as before. After the dry etch step, the photoresist remains on the wafer. The resulting sidewall profile of the nitride is suitable for metal liftoff because the nitride etch undercuts the photoresist. In this way, delta gates ranging from 0.25 to 0.50 μm have been defined. Experiments are ongoing to determine if this process gives improved performance and manufacturability compared to our existing half micron optical process.

DC RESULTS

The DC results of this optical T-gate process compare well with e-beam defined gates. On average, $G_{m,max}$ increased by 5% (to over 400 mS/mm) and $I_{d,max}$ increased by 5-10% (to 570-600 mA/mm). The pinchoff voltage tends to be around 100 mV more positive (-900 mV) which may be related to the slight amount of damage introduced during the dry etch of the trunk feature. Breakdown voltage (BV_{gd} ~ -20 V) and other DC parameters are roughly equivalent, except their standard deviations within wafer have been reduced by over a factor of two through utilization of the optical process. These improvements are attributed to the earlier application of the nitride passivation, which protects the ohmics and wide recessed region from processing steps that can damage the surface.

RF LOAD PULL RESULTS

Load pull measurements have consistently resulted in more output power at high drain bias with the optical process compared to the standard process. CW on-wafer load pull measurements were taken at 1.9, 10 and 18 GHz on 300 and 600 μm-wide devices with drain biases ranging from 6 to 15 V. Three different load pull setups were used to verify results and measure at different frequencies. From 6 to 10 V drain bias, the two processes provide similar output power characteristics. Above 10 V drain bias, the optical process gives higher output power while the output power of the standard e-beam process begins to degrade (Figure 3). The highest observed power density at 10 GHz (recorded at P1dB compression and peak PAE) was 1.80 W/mm with a PAE of 56%, and 13.8 dB gain which occurred at a drain bias of 13 V (Figure 4). The saturated output power was 1.9 W/mm. We believe this represents the highest reported power density from a GaAs pHEMT device.

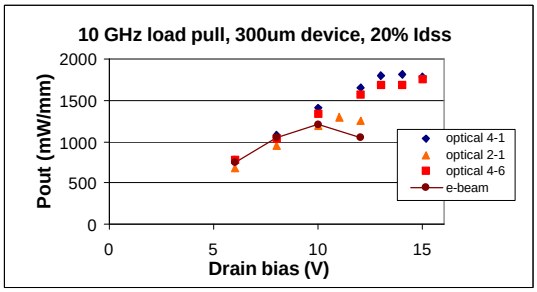

Figure 3. Load pull measurements at 10 GHz showing Pout at max PAE vs. Vd. At higher drain bias the new optical process has higher Pout than the standard process.

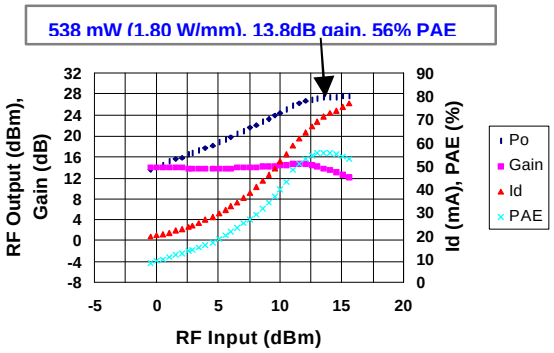

Figure 4. Load pull measurement at 10GHz of 300µm device. Tuned for power.

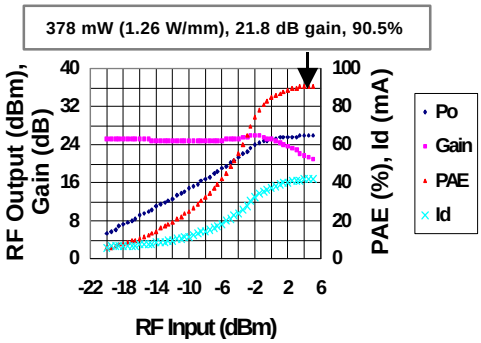

Figure 5. Load pull at 1.9 GHz of a 300µm device. Tuned for efficiency. Power tune gave over 2.0 W/mm.

Load pull testing at 1.9 GHz resulted in 2.02 W/mm with 22.8 dB gain and a PAE of 74%. By optimizing for efficiency, a PAE of 90 % was also obtained at 1.9 GHz (Figure 5). Table I shows a sample of the load pull results taken at different set ups, device sizes and frequencies. These numbers represent the best performers from each lot, and the variation within each lot was about 0.1 W/mm. Earlier lots (numbers 1-3 in Table I) run with the optical process consistently gave peak power outputs of 1.3 - 1.4 W/mm at 10 or 11 V which were improvements over the standard e-beam processed devices (1.1 to 1.2 W/mm). The most recent lot, #4, had small process changes which increased its breakdown voltage. This plus improved load pull tuning at higher drain biases enabled it to achieve the highest output powers. Reported power densities for GaAs pHEMTs have typically been close to 1.0 W/mm [4] although this is usually measured at lower drain biases (in the 8-10 V range). To our knowledge, the previously reported highest power output density was 1.6 W/mm at 2.0 GHz with a gain of 12 dB and biased at 12 V [5].

RF MMIC TESTING

In MMIC testing at X-band, full wafer RF probe demonstrated both high yield (over 90%) and increased output power with the optically processed wafers on a circuit with over 11 mm of gate periphery. These tests were done on a TriQuint standard product, TGA9083 (Figure 6), which is designed to give 8W at 9V and can deliver a maximum power of about 10 W. One optically processed MMIC device was fixtured for pulsed power testing and produced over 13 W of power (1.17 W/mm) with 17.2 dB gain and 38% PAE at 9.5GHz and a drain bias of 12 V. This was an older wafer (3-1) that reached only 1.31 W/mm on a 300µm discrete FET at load pull. MMIC parts from the most recent lot (which gave 1.80 W/mm at load pull) are being prepared for pulsed testing. The standard processed parts degrade or blow up before reaching these power levels. Note this performance was obtained on a circuit that was designed with standard gate models. It is believed that even better circuit performance can be obtained by redesigning with new optical T-gate FET models.

CUTOFF FREQUENCY

Measured cutoff frequencies (F_t) of the optical process are lower than the e-beam defined gates by about 7 GHz. The slightly larger gate length, parasitic capacitances, and possibly the shape of the T-gate are believed to be responsible. A reduced gate length process is in development for circuits that operate above 30 GHz. Varying parameters such as trunk height, cap width and the profile of the nitride etch may improve F_t. Improvements in the optical lithography and/or the dielectric etch may also increase F_t. If necessary, an e-beam or deep UV stepper can be used to write smaller trunk features. There would still be the improvement in throughput [6] and hopefully the same improvement in power density.

TABLE I
SUMMARY OF LOAD PULL RESULTS

Lot-wafer#	Tuned for:	Freq. (GHz)	Load pull setup	Device size (µm)	Pout at max PAE (dBm)	Gain at max PAE (dB)	max PAE (%)	Drain bias (V)	Power density (mW/mm)
1-5	pwr	10	A	600	29.23	12.7	54.4	11	1.40
"	eff	10	A	600	25.20	11.5	64.7	6	0.55
2-1	pwr	10	A	600	28.99	12.7	55.1	10	1.32
"	pwr	18	A	600	28.66	8.4	49.3	10	1.22
3-1	pwr	10	B	300	25.93	12.8	49.9	12	1.31
4-6	pwr	10	B	300	27.05	13.6	56.1	13	1.69
4-1	pwr	10	B	300	27.32	13.8	55.8	13	1.80
"	pwr	1.9	C	300	27.82	22.8	74.3	12	2.02
"	eff	1.9	C	300	25.76	21.3	90.0	10	1.26
std process	pwr	10	B	300	25.57	13.7	51.8	10	1.20
Ref [4]	pwr	10	-	800	29.3	11.4	56.5	9	1.06
Ref [5]	pwr	2	-	2500	36	12.0	62	12	1.60

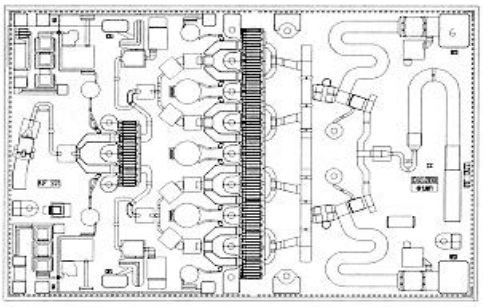

Figure 6. Layout of 11mm MMIC (TGA 9083). Die size is 4.5x3x0.1mm. Pulsed power test gave over 13 W at X-band with the new process.

DISCUSSION

The improvement in RF performance is believed to be due to the earlier surface passivation and possibly the surface preparation just before gate nitride deposition. Since the pHEMT is a surface device, proper treatment of the surface is critical. Huang et al [7] reported on the "parasitic gating" problem wherein surface states in the wide recess region trap electrons and impede the RF performance. By passivating with nitride immediately after wide recess, the effect of surface states and traps is reduced. The surface no longer sees the harsh resist strips associated with gate and first metal liftoff. It is possible that passivating the GaAs surface as the very first process step may prove to be even more beneficial.

Initial reliability tests are encouraging in that the devices perform as well as our standard pHEMTs in DC life tests at 8V and a channel temperature of 320°C. More extensive reliability tests at different temperatures and drain biases are underway. It is especially critical to determine the lifetime of these devices when operated at elevated drain biases where the greatly improved power output is observed. Thermal issues may become more significant at the higher power densities and can be addressed in a redesign if necessary.

CONCLUSION

By switching to a dielectrically defined T-gate, record output power densities were achieved. The improved RF performance offers higher output power density resulting in better performing circuits with smaller die size. Power densities of close to 2 W/mm make this process very attractive for high power amplifiers up to 20 GHz, and represent a significant advance for GaAs pHEMT technology. Potential applications include high power airborne phased array radar and L-band wireless base stations. A similar process with smaller gate lengths will extend the operating frequency to 40 GHz and hopefully maintain the performance improvements. The dielectrically defined T-gate process also offers several inherent advantages from a manufacturing standpoint. The higher throughput and yield offer obvious cost savings, while the reduced variability of DC parameters offers tighter process control.

ACKNOWLEDGEMENTS

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