Effect of Intentional Surface Oxidation on Power Performance in Planer Type AlGaAs/GaAs MESFET

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Abstract

The purpose of this study is to improve the output power (Pout) and 3rd-order intermodulation distortion (IM3) of planer type GaAs power FET, which is used for RF power amplifiers for base stations of digital wireless communications systems. We focused on the GaAs surface state and tried to improve the FET performance by intentional GaAs surface oxidization just prior to SiN cap deposition. Thermal or plasma oxidation has been found to improve Pout and IM3 characteristics. Distinct improvement of FET performance was observed in intentionally oxidized FET, and the highest Pout = 34 dBm and Pout(@IM3=-55dBc) = 23 dBm was measured on plasma oxidized FET with Wg = 5.2 mm.

1. Introduction

The output power (Pout) and 3rd-order intermodulation distortion (IM3) are affected significantly by the parasitic resistance between the source and drain region. Though the gate recess structure is effective to improve the FET performance, it is difficult to fabricate the recessed FET in high reproducibility. So, we have employed the planer structure, in which the parasitic resistivity is compensated by n^+ and n' ion implantation. [1]

Another important factor that affect the FET performance is the carrier traps existing at GaAs surface. The traps capture electrons and reduce the Ids under the RF input signal. This leads to degradation of Pout and IM3. Moreover, GaAs surface usually has some "native" oxide, which grows even in air at room temperature and changes following reaction, $As_2O_3+2GaAs \rightarrow Ga_2O_3+4As$ [2]. This reaction also changes the GaAs surface state.

For reproducible manufacturing of FET, the GaAs surface state should be controlled well enough. The well controlled surface with less electron traps also promise the high performance of FET.

In this study, we have introduced "intentional" surface oxidation. The optimized process of oxidation and SiN cap film deposition was the key point to improve the FET performance. The results of GaAs surface analysis and RF performance measurements will be described in detail. We also report about the improvement mechanism.

2. Fabrication process

Figures 1 and 2 show the cross-sectional image of FET and its fabrication process flow, respectively. The substrate has pulse-doped GaAs channels and an undoped GaAs/AlGaAs cap layer, which is covered by a PE-CVD SiN thin film. The n+ and n' implanted regions were formed by Si+ ion implantation and rapid thermal annealing (RTA). The SiN anneal cap remains after RTA to passivate the GaAs surface. Ohmic and gate metals were formed by a conventional EB-evaporation and lift-off processes.

We have tried to cover the GaAs surface with some amount of stable Ga_2O_3 in expectation of reduction in the surface traps [3]. The intentional oxidation just prior to SiN cap deposition increases the As_2O_3 and Ga_2O_3 mixture on the GaAs surface. During the RTA, instable As_2O_3 changes into stable Ga_2O_3 and elemental As diffuses out through the SiN film. The SiN film should be tough enough so that the

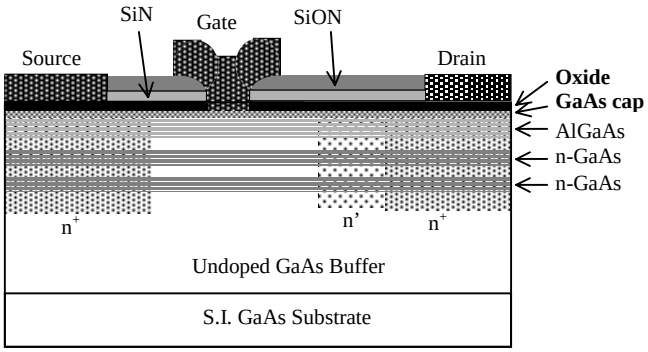

Figure 1 Cross sectional view of planer type AlGaAs/GaAs MESFET

1. Epitaxial growth
2. Mesa etching for isolation
3. Anneal cap deposition
4. Ion implantation(n+, n')
5. Activation anneal(RTA)
6. Ohmic & Gate Metals
7. 0th via hole
8. Metalization(Level 1)
9. 1st via hole
10. Metalization(Level 2)
11. Passivation

Figure 2 Fabrication process flow of power FET IC

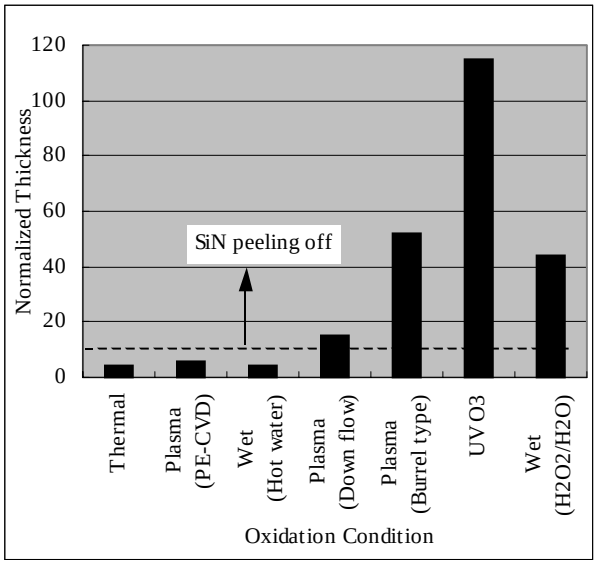

Figure3
The oxidation condition and thickness of the formed oxide.
Thickness of the oxide were evaluated by ellipsometry and normalized by that of native oxide.

As can go through without SiN peeling off during RTA.

The results of various kinds of oxidation processes are shown in Figure 3. The oxide thickness was measured by the ellipsometry and normalized by the thickness of native oxide. For example, in case of using UV-O_3 or H_2O_2/H_2O, the normalized thickness became larger than 10, which made the SiN peel off. Though just dipping in hot water gave the thickness smaller than 10, it varied from 0 to 4.

Finally, following two methods were found promising. One is thermal oxidation, that is the hot-plate heating in air. The other is plasma oxidation for 20 seconds in the PE-CVD chamber, in which the SiN film is deposited consecutively. The plasma oxidation made the operation easier than thermal one and was expected to reduce the surface contamination.

Figure 4 shows the cross-sectional TEM images. Though the oxide layer cannot be distinguished from SiN thin film, the extent of oxidation can be estimated from the thickness of the top GaAs cap layer that remains without being oxidized. In case of native oxide, the remaining GaAs thickness was almost same as that of starting material, and the thickness of oxidized GaAs was less than 5 Å. On the other hand, those of thermal and plasma oxidation were about 25 Å and 20 Å, respectively.

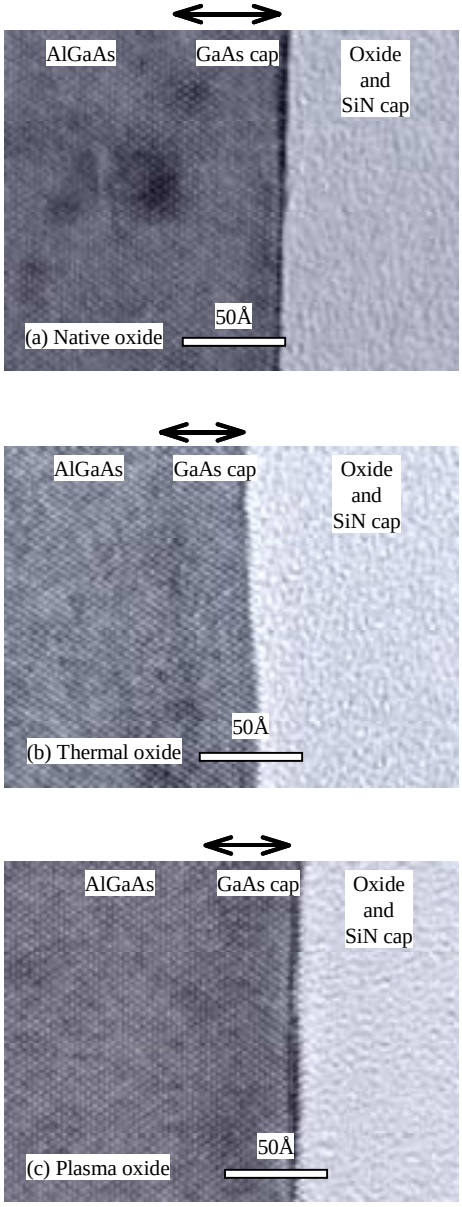

Figure 4
Cross-sectional TEM images of the GaAs surface with
(a) native oxide, (b) thermal oxide, (c) plasma oxide
The bright regions on right are mixture of oxide and SiN cap. They can not be distinguished from each other, because they are both amorphous.

Table 2 Oxidation condition and thickness of oxidized GaAs cap

Oxidization condition	Native	Thermal	Plasma
Thickness of **oxidized** GaAs	<5 Å	~25 Å	~20 Å

3. Performance of fabricated FET

At first, the I-V curves were measured under the DC or pulsed bias to evaluate the trap elimination effect by intentional oxidization. The pulse interval was 1 μsec. Under DC bias, the drain current of FET with only native oxide was larger than that of intentionally oxidized FET especially

at the knee voltage(Ids@Vknee) (Figure 5(a)). On the other hand, under pulsed bias they showed a reversed relationship as shown in Figure 5(b). Ids of FET with only native oxide became smaller than that of intentionally oxidized FET. This reduction in Ids@Vknee resulted in the reduction in Pout as shown bellow.

Pout and IM3 characteristics are shown in Figure 6. the measured devices had a gate length of 0.7μm and gate width of 5.2mm. The measurement conditions were Vd=8V and Id=400mA. Both Pout and IM3 characteristics are apparently improved by intentional oxidization. While P1dB of FET with only native oxide is 32.5dBm, that with the intentional thermal oxide is increased up to 33.0dBm. Moreover, the plasma-oxidized FET shows the highest P1dB of 34.0dBm.

For further investigation on IM3 characteristics, the IM3 contour was measured. On the Smith chart, IM3 was measured at 63 points and the IM3 contour was determined (Figure 7).

The Plasma-oxidized FET shows an apparently larger IM3 contour circle compared to the thermally oxidized FET. Especially the contour of IM3=-60dBc was observed only in case of the plasma oxidized FET. This means plasma-oxidized FET can provide large margin for the PA module designer.

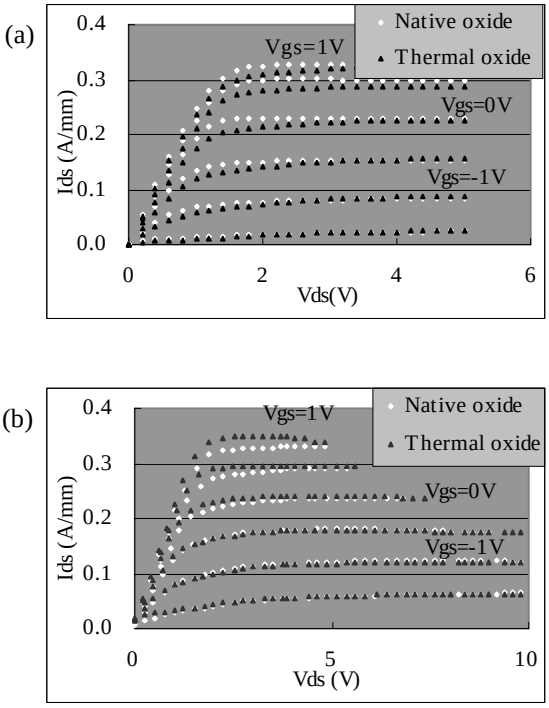

Figure 5
I-V curves of FET with only native(white symbol) or thermal(black symbol) oxide.
(a) DC bias was applied for the FETwith Wg=125um and Lg=0.7μm.
(b) Pulsed bias was applied with pulse interval of 1usec for the FET with Wg=0.5mm and Lg=0.7μm

4. Investigation in mechanism

The mechanism of RF performance improvement by intentional oxidation is assumed as follows.

From TEM observation it was clarified that the thickness of native oxide is very thin. This thin oxide implies that large amount of unbonding GaAs surface atoms, which acts as carrier traps, is remained. In contrary, thermal and plasma oxidation have about 25 Å of oxide and assumed to have less unbonding atoms. This is thought to improve the FET performance under RF input signal.

On the other hand, though the plasma oxidized FET had thinner oxide thickness than the thermally oxidized FET, the former showed the higher RF performance than the latter. This high RF performance of the plasma oxidized FET possibly attribute to the quality of Ga_2O_3 layer.

5. Conclusion

In the fabrication of planer type power FET, the intentional oxidation process was introduced just prior to the deposition of anneal cap to improve Pout and IM3. Plasma oxidized FET showed the highest performance of Pout=34dBm and Pout(@IM3=-55dBc)=23dBm. It was thought that the improvement of FET performance by

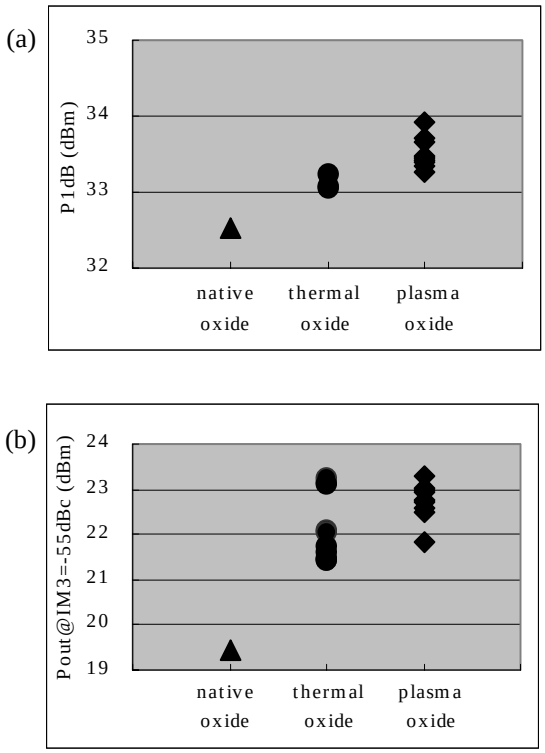

Figure 6
Pout and IM3 characteristics measured on the FETs with Wg=5.2mm and Lg=0.7μm
(a) Pout when it becomes smaller than the value estimated from linear relationship with Pin by 1dB: P1dB
(b) Pout when IM3 = -55dBc : Pout@IM3=-55dBc
Measurement condition was Vd=8V, Id=400mA.

intentional oxidation may be attributed to the reduction in carrier traps at the GaAs surface. Further analysis is necessary to clarify the relationship between the origin of traps and oxidation process.

References
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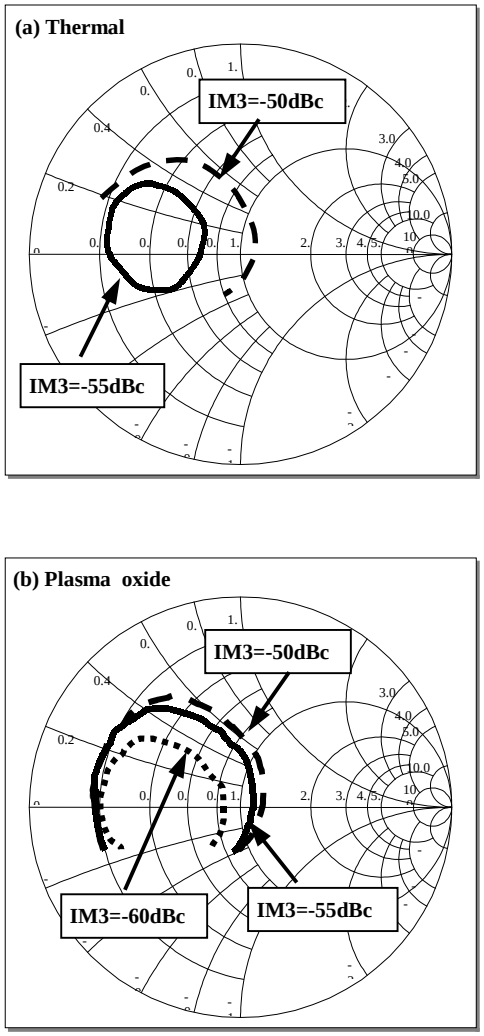

Figure 7
IM3 contour when Pout=20dBm
(a) Thermally oxidized FET
(b) Plasma oxidized FET
Measurement condition was Vd=8V, Id=400mA
The dashed line is contour of IM3=-50dBc, the solid line is of 55dBc and the dotted line is of 60dBc.