A Highly Uniform, and High Throughput, Double Selective pHEMT Process Using an All Wet Etch Chemistry

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Abstract

Epitaxial material structure and wet-etch methods have been developed for a Double Selective Recess (DSR) power pHEMT process at X-band. Seven citric acid based etch solutions and eight different epitaxial material structures with AlAs etch stop layers have been investigated. The optimized epitaxial material produces devices with DC and RF performance that are similar to the ones fabricated with Selective First Recess (SFR) only process but with ≥3 times better threshold voltage uniformity. Ellipsometry technique and an etch-monitor structure have been utilized to accurately determine the etch rate. This has enabled us to minimize the ungated recess width during the gate over-etch step.

INTRODUCTION

Gate recessing is one the most important process steps in the fabrication of pHEMT devices. The non-selective gate recess method results in poor uniformity of the threshold voltage of devices with various sizes within a chip and across the wafer. This is especially true for high performance pHEMTs with a threshold voltage sensitivity of 7-10 mV/Å of etch depth.

Selective gate recess using dry etch methods and AlGaAs, AlAs, and InGaP etch stop layers have been reported in the literature [1-2]. Dry etching requires a careful balance between the GaAs or AlGaAs etch rate, selectivity with respect to the etch stop material, critical dimension change due to resist erosion, and damage to the underlying Schottky layer material. These conflicting requirements are often hard to satisfy in a liftoff based Tee-gate structure.

Selective gate etch using wet etch chemistry and AlGaAs or InGaP etch stop layers have been reported in the past. However, data on optimization of wet etch solution and epitaxial material, as well as DC and RF Yield have been lacking.

EPITAXIAL LAYER STRUCTURE IMPACT ON DEVICE CHARACTERISTICS

A schematic cross sectional view of a generic DSR structure is shown in Figure 1. The main features of this structure are as follows. 1.) A top GaAs N+/N layer with thickness of d_1, which is etched away during the first recess selective etch step. 2.) The first AlAs etch stop layer.

3.) The second GaAs N layer with thickness d2, which is etched away during the selective gate recess etch stop.
4.) The second AlAs etch stop layer, AlGaAs Schottky layer, channel, etc.

AlGaAs Schottky / Channel / Super-lattice Buffer

Semi-insulating GaAs Substrate

Top N^+ / N GaAs Contact Layer (d_1: 100-900 Å)
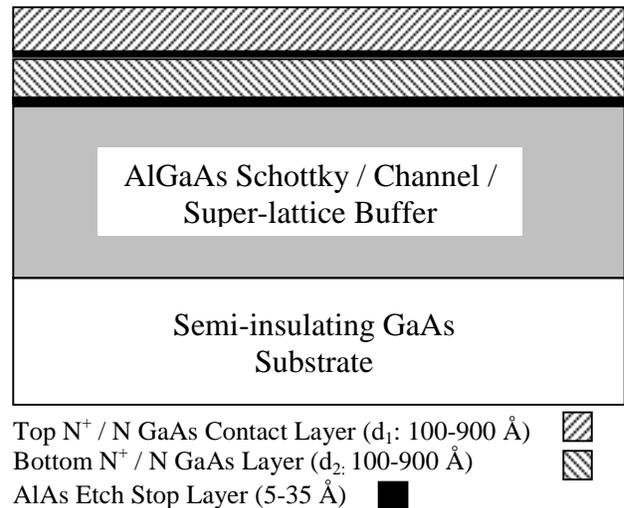Bottom N^+ / N GaAs Layer (d_2: 100-900 Å)
AlAs Etch Stop Layer (5-35 Å)

Figure 1. Generic DSR epitaxial layer structure

We have studied epitaxial layer structures across the practical range of d1 and d2 thickness. At first, we simply inserted a second AlAs etch stop layer to the base-line SFR material at a depth that gate would nominally be located. This resulted in devices with severely degraded Maximum Current (Imax) and Source Resistance (Rs). To understand the reason for this phenomenon, we consider the equivalent circuit diagram shown in Figures 2-3. Each AlAs etch stop layer creates an electrical barrier to current flow. It can also impede the penetration of ohmic contact during the alloy process. Referring to Figures 2-3, increasing the doping level in the bottom GaAs layer will increase Imax. Source resistance will also be reduced. However, the breakdown voltage will suffer due to the high doping. These restrictions do not apply to the top GaAs cap layer. Having studied the two dimensional electron gas sheet charge densities of 2.6 to 3.2 x10^{12} cm^{-2}, and thickness ranges indicated in Figure 1, the following design guidelines have been established.

The GaAs cap layer and first AlAs etch stop layer should be doped as high as possible. 2.) The total thickness of top and

bottom GaAs layers should be minimized subject to achieving the desired mesa sheet resistance. 3.) The channel sheet charge should be maximized subject to the breakdown voltage requirements.
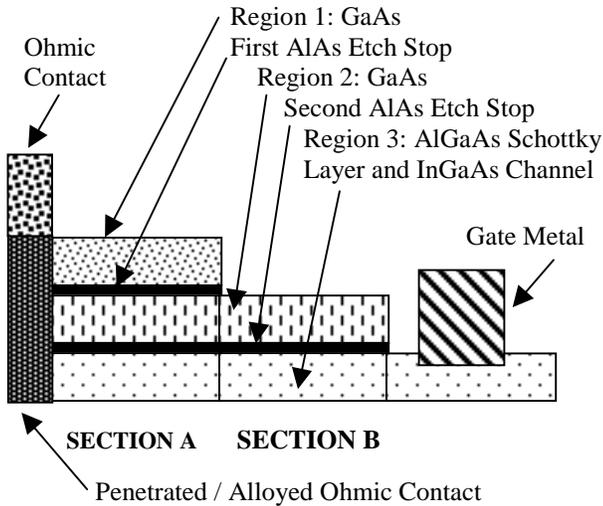

Figure 2. Schematic cross section of a double-recessed and double-selective (DSR) pHEMT.
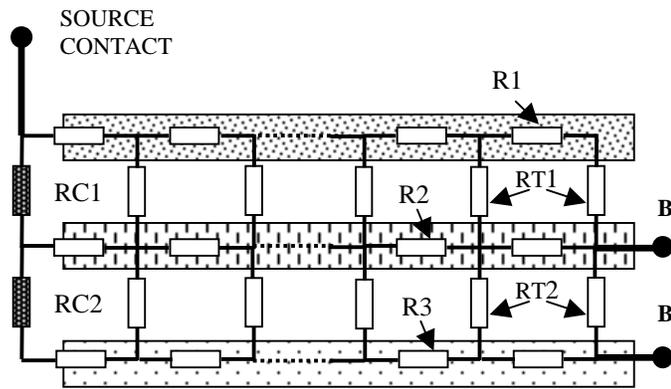

Figure 3(a). Simplified equivalent DC circuit-model of section A shown in Figure 2. RT1 and RT2 are the tunneling resistances due to the first and second AlAs etch stop layers.
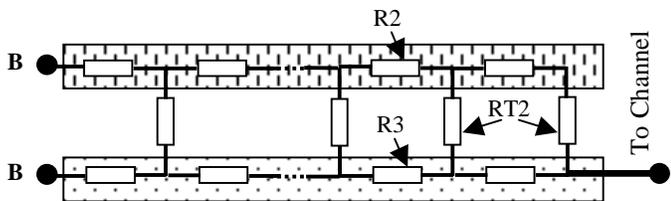

Figure 3(b). Simplified equivalent DC circuit model of section B shown in Figure 2.

ETCH SOLUTIONS, UNDERCUT, AND ETCH RATE DETERMINATION USING AN ELLIPSOMETER

Citric acid based etch solution with high selectivity with respect to AlGaAs (≥25% Al) has been reported in the literature [3]. We call this solution the Base Line Buffered (BLB) type. The etch solutions that we have studied are listed in Table 1. All dilutions were made in DI-H2O. It is important to note that although only the BLB solution is selective with respect to AlGaAs (≥25% Al), all of the solutions listed in Table 1 etch GaAs selectively with respect to AlAs. The undercut ratio in Table 1 is defined as the width of the undercut during over-etch step divided by the over-etch depth that would have occurred if the second AlAs etch stop layer had not been present.

Table 1. Etch rate of various citric acid based etch solutions for GaAs and

Etch Type	Dilution Ratio	pH	Temp. (C)	Rate (Å/Min)	Undercut Ratio
BLB	NONE	6.4	20	1500	1.8
1	NONE	2.14	21	516	1.9
2	NONE	4.5	21	672	1.4
3	1:1	2.4	20.5	258	1.8
4	1:1	4.5	20	354	1.4
5	1:2	2.4	20	162	1.7
6	1:2	4.7	19	264	1.5

In practice, one should chose an etch solution that will result in a meaningful amount of etch time during the critical gate etch step such that a few seconds of error in etching would not impact the device parameters. It should be mentioned that all of the etch solutions in Table 1 have high "activation" energy and as such they are quite sensitive to temperature. A successful implementation for manufacturing requires temperature control to ≤1 ^{o}C.

One of main issues facing selective wet etch at the gate recess step is the percentage of over-etch and the ensuing lateral undercut. This undercut region, which we refer to as the ungated recess, is not desirable for some applications. Figure 4 shows a TEM cross section of a DSR device with ~30% over-etch using the BLB solution. Control and minimization of the ungated recess requires an accurate determination of the etch rate. We have used a GaAs/AlAs material stack etch monitor with 15 or higher periods. The thickness of GaAs and AlAs layers of each period are the same as the ones in device wafers during the gate etch step. One starts with a rough estimate of the etch rate, and etches the first GaAs layer with ~20% over-etch. We utilize a standard, single wavelength ellipsometer to confirm that the GaAs has been etched away and etching has stopped on AlAs. This method has been utilized in the past for detection of a few Angstrom of oxides and other contaminants on a GaAs substrate [4-5]. Next, we reduce the over-etch percentage in small steps, e.g.,

5%, until the ellipsometer can verify that the GaAs layer has not been completely etched off. The net result is that one can measure the etch rate to an accuracy of ≤5%. Thereby, over-etch time can be minimized.
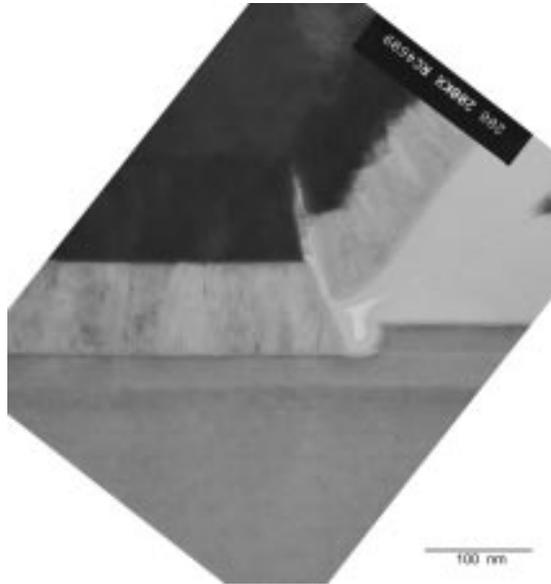

Figure 4. TEM cross sectional view of a DSR device with ~30% over-etch.

DEVICE RESULTS

We have fabricated high power (8-10 W) X-band power amplifiers using DSR method. Even in the engineering mode of process development, DC yield of ~74% is observed for ~30 wafers, with one lot having a yield as high as 84%. The main attribute of the DSR method, as far as the circuit is concerned, is excellent threshold voltage uniformity. This is shown in Figure 5. RF performance of a DSR chip is shown in Figure 6. Accelerated DC life test has been performed on devices made using DSR process. The DC mean time to failure is quite similar to the devices made using SFR only process. The DC failure criterion is defined as a 20% reduction of drain current Id. The bias conditions for DC reliability test are Vds=8.0 V, and Id=150 mA/mm.

CONCLUSIONS

A double selective recess method, using AlAs etch stop layers for both first recess and gate, has been shown to offer excellent threshold voltage uniformity and performance. Factors that impact the design of the epitaxial layer have been explored. It was shown that control of the ungated recess region requires an accurate determination of the etch rate during the gate recess process step. A method based on a

special etch-monitor structure and ellipsometry has been introduced for accurate measurements of etch solutions rate.
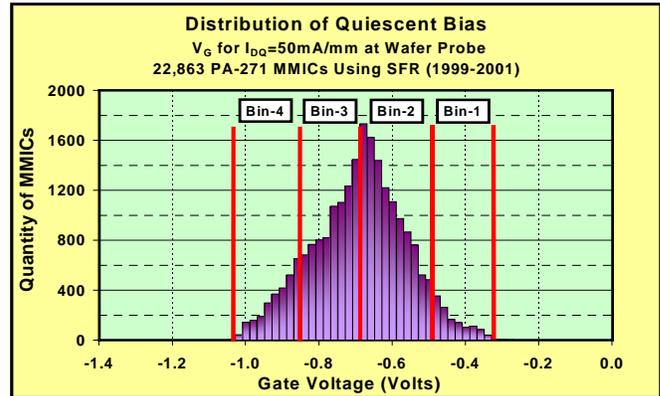

Figure 5(a). Gate Voltage Setting Distribution for a Selective First Recess Only (SFR) Power Amplifier Circuits. Data for 22863 circuits is shown.
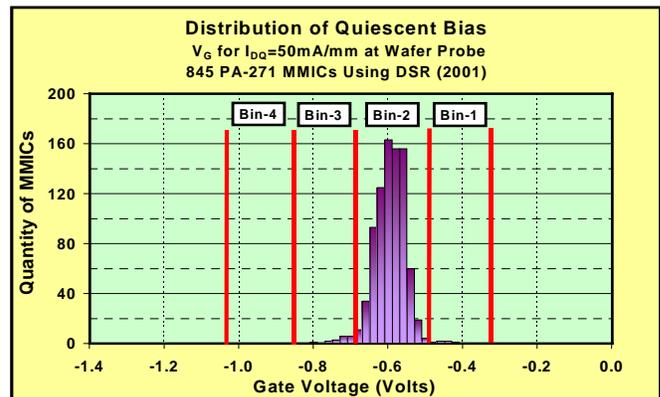

Figure 5(b). Gate Voltage Setting Distribution for a DSR Power Amplifier Circuits. Data for 845 circuits is shown.
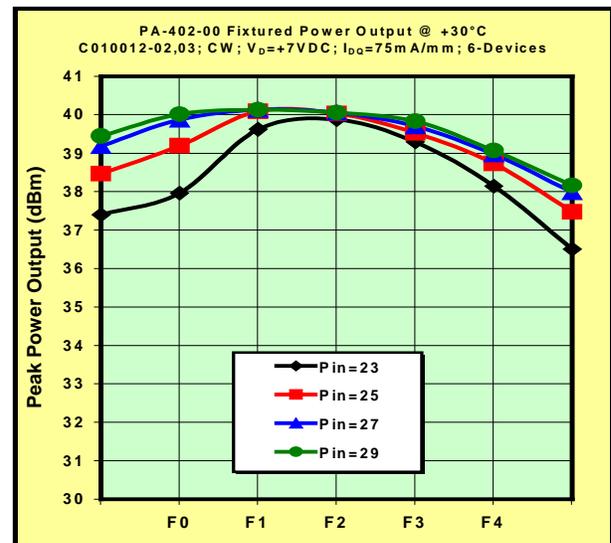

Figure 6. RF performance of X band power amplifiers fabricated with DSR method. Vd=7 V, Idq=75 mA/mm. Input powers of 23, 25, 27, and 29 dBm are shown.

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