Capability and Cycle Time Improvements in Nortel Networks' Substrate Via Fab

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Abstract

Market requirements for increased RF performance, higher power and improved thermal dissipation have necessitated optimisation activities, not only in frontside circuit processing, but also in the area of backside via processing. Within Nortel Networks, both the establishment of a new Full Power HBT (FPHBT) product line and the demand for smaller via dimensions have driven the development of processes to deliver new capabilities and improved cycle time in Nortel Networks Substrate Via (SVia) Fab.

This paper focuses on new process implementation, from challenges encountered thinning FPHBT wafers to via formation using a resist-based mask process with a Trikon Omega® 201 ICP etch system. Limitations with thinning new FPHBT wafers using a rosin-based resin process and with utilization of the standard hard mask process to accommodate reduced via sizes will be explained. In addition, the improved manufacturability and cycle time reduction by the establishment of a resist-based via etch process will be reviewed.

INTRODUCTION

Since its inception in 1994, Nortel Networks' SVia facility has been backside processing GaAs wafers to fulfil MESFET [1] and HBT [2] product requirements. During the majority of this period, backside requirements consisted of the thinning of wafers to 100µm for devices requiring through vias, and 185µm for devices without vias. Via dimensions were 80µm in diameter or 80µm x 30µm.

Of note, the frontside topography of standard product wafers consists of 4-6µm of passivated, evaporated gold with airbridge interconnect for MESFET, and polymer dielectric for HBT. A pictorial representation of the standard backside process flow is indicated in Figure 1. The backside processing of both the MESFET and HBT wafers is initiated with the bonding of wafers to sapphire carriers. The bonding process utilizes a spin-on rosin-based resin adhesive. The resin is spun on, then hotplate cured onto a 1mm-thick carrier to a thickness of ~10.5µm. Wafers are bonded to the carrier and adhesive utilizing heat and pressure. After bonding, wafers are thinned to the required thickness using a batch grinder system, followed by a wet chemical polish. Wafers not requiring through vias are simply backside metalized with a sputtered Ti/Au seedlayer followed by electroplated gold. Wafers requiring though vias receive a 5µm deposition of PECVD SiON and via lithography patterning. Pattern transfer into the SiON is achieved with a BHF etch. Once the resist pattern is stripped, the vias are etched into the substrate with an RIE etcher. The remaining SiON mask is stripped off and the wafers are backside metalized. In via processing, a layer of Ti is applied into the vias to minimize solder wicking. The Ti is sputtered onto the wafer and the wafer is coated with resist. The wafer is flood exposed and developed leaving resist in the vias. The Ti is etched off the wafer surface in a BHF solution and the resist is stripped.

After backside metalization, wafers are dismounted by heating the wafer and carrier above the adhesive melting point and physically separating the carrier from the wafer. Final wafer cleaning is achieved with a xylene soak and an O plasma descum. A cross-sectional view of a standard via is illustrated in Figure 2.

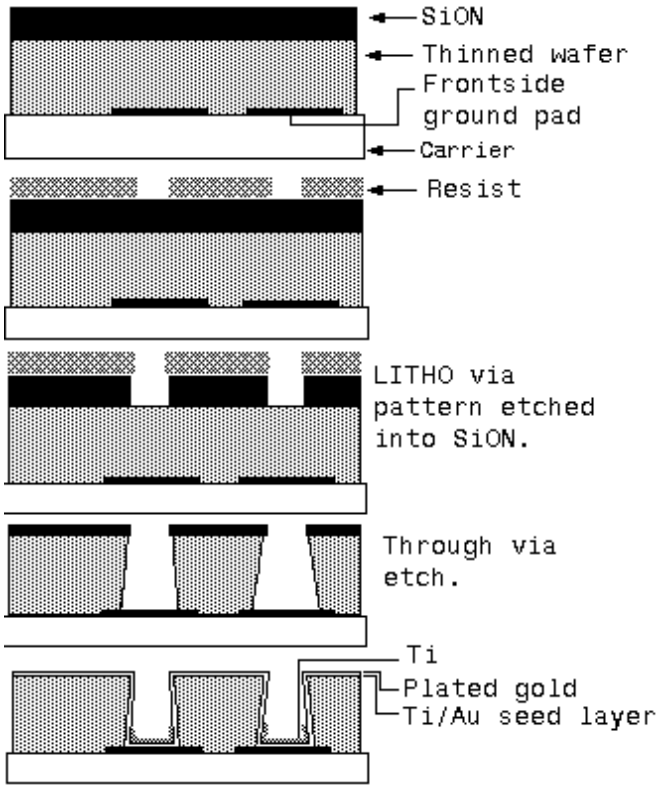

Figure 1: The standard through via etch flow.

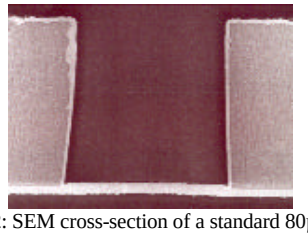
Figure 2: SEM cross-section of a standard 80µm via.

FABRICATION ISSUES FROM NEW REQUIREMENTS

In March 2000, backside processing of a new FPHBT process was required. The frontside topography of these wafers consists of 8µm of passivated electroplated Au. The standard requirements for thinning were maintained, 100µm for devices requiring vias and 185µm for devices without vias. However, via dimensions were reduced to 40µm in diameter.

Design requests to further shrink via dimensions, thus enhancing product performance, led to the investigation of mini vias within the facility. The reduction of the backside through vias to 7µm x 10µm was requested with the existing through via process flow. These requirements posed significant processing challenges, described below.

A) Full Power HBT Process

Attempts to process the FPHBT product using the rosin-based resin adhesive was found to create a yield issue when thinning the wafers with our batch grinder. In the first attempt, 2 of 17 wafers processed were damaged during thinning. Typical grinding failures are shown in Figure 3.

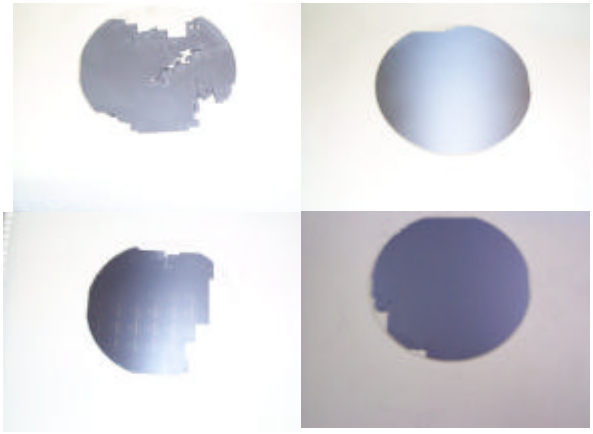

Figure 3: FPHBT wafers damaged during resin adhesive qualification

Attempts with a modified resin process, using HMDS vapour prime and a thicker resin coat (~15 +/- 2µm), achieved only slightly better yield results. As indicated in Table 1, the modified process was successful in thinning FPHBT wafers to 185µm, however yields when thinning wafers to 100µm and 50µm were unacceptable. In addition, frequent re-work after bonding was required due to cracks in the resin at the edge of the wafer. Edge preparation, to remove passivation and metal delamination, was found to be critical for the reduction of rework.

TABLE 1
MODIFIED RESIN RESULTS FOR FPHBT QUALIFICATION.

# of Wafers	Process	Thickness	Yield
13	FPHBT	185µm	100%
19	FPHBT	100µm	74%
8	FPHBT	50µm	75%
9	MESFET	50µm	100%

Upon final analysis, the root cause of wafer breakage during grinding was attributed to three factors: the poor adhesion of the resin to large sections of plated gold, resin adhesion sensitivities to FPHBT edge preparation, and the loss of resin strength due to embrittlement of the film from excessive temperature exposure.

B) Mini Vias

Attempts using the standard SVia process to etch mini vias were found to be inadequate using the alignment tolerances established by the design group. The mini via designs required a 7µm X 10µm via alignment to a 20µm X 30µm pad using 50µm thick substrates. An example of cross-sectional misalignment experienced during the evaluation is shown on the right of Figure 4.

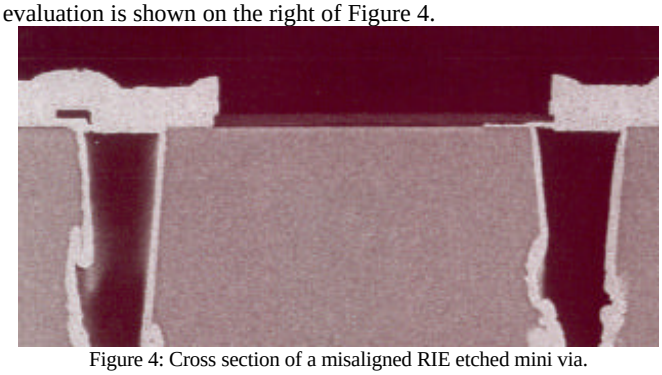

Figure 4: Cross section of a misaligned RIE etched mini via.

Three factors impacted the successful implementation of mini vias using the standard process. First, a run out problem prevented accurate alignment of the via pattern during contact alignment to the frontside devices, as seen in Figure 5.

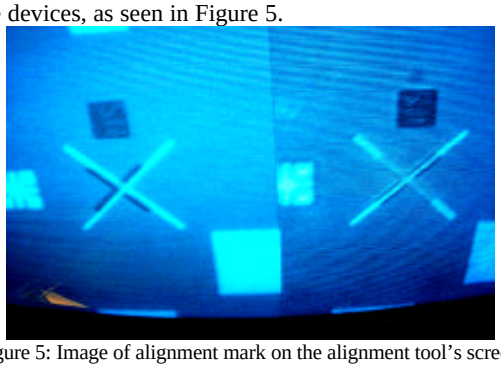

Figure 5: Image of alignment mark on the alignment tool's screen.

Using process segregation, it was determined that run out values increased dramatically after the SiON deposition, and the run out was found to be inconsistent in magnitude and direction from run to run. The second factor was the bias increase in via dimension from the initial lithography patterning to the final through via. When comparing mask to frontside contact dimensions, via sizes increased by an average of 10µm during the SiON etch and GaAs dry etch. The third factor was the via profile itself. The final through via profile is re-entrant, resulting in a larger via dimension at the frontside surface compared to the backside surface. All these factors resulted in unacceptable mini vias that caused shorts within the device, as seen in Figure 6.

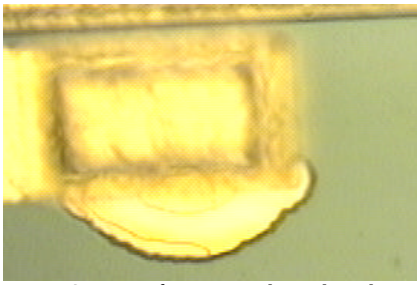

Figure 6: Image of an oversized, misaligned via.

FULL POWER HBT PROCESS IMPROVEMENTS

A) Thinning, Wafer Dismount and Cleaning

The yield when thinning FPHBT wafers was improved with the use of a thermoplastic adhesive. The wafer is bonded to a perforated sapphire carrier using the standard process bonding tool. The adhesion is not comprised by edge preparation or minor bubbles in the film. Yield figures to date, are shown in Table 2.

TABLE 2
YIELD AT GRIND USING THERMOPLASTIC ADHESIVE

# of Wafers	Process	Thickness	Yield
30	FPHBT	185µm	100%
125	FPHBT	100µm	100%

A major limitation of using the thermoplastic adhesive had been final wafer cleanliness and dismount capability. The initial dismount and final cleaning processes had utilized a N-methyl-2-pyrrolidinone-based post-etch residue remover. This method was characterized by long dismount times and thermoplastic residue problems (Figure 7).

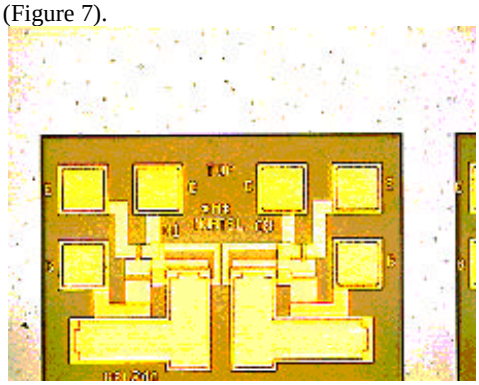

Figure 7: Thermoplastic residues after dismount and clean

To reduce dismount time and residues, new chemical processes were introduced. The current dismount method uses GenSolve500® for bulk removal of the thermoplastic adhesive and GenSolve550® to clean and remove remaining residues from the wafer surface. Ultrasonic cleaning is not used in the dismount process. Use of GenSolve500® has reduced dismount times by 50%. Additional experiments have shown that an increase in the dismount chemical's temperature from 65ºC to 120ºC will decrease wafer dismount times by an additional 60%. In addition, the density of the perforations, and size of the perforation exclusion zone at the edge of the carrier are important variables in reducing dismount times. A change in carrier design from a 6.6mm to a 2.4mm perforation exclusion zone at the edge of the wafer has resulted in a 50% reduction in wafer dismount time. The use of GenSolve550® has reduced die visual yield loss due to foreign material from 10% to 6% on thinned, plated FPHBT product.

B) Via Process Issues with Thermoplastic Adhesive

Further difficulties were experienced when processing product with backside vias. During resist strip and lithographic rework, an insoluble residue is created from the reaction of acetone with the exposed thermoplastic in the carrier perforation openings. This reaction has been limited by the use of a track spray dispense of acetone and IPA in place of the previous immersion resist strip.

The frontside SiON is susceptible to attack during BHF etches, since openings in the adhesive can be formed by carrier perforations cutting into the thermoplastic during the bonding process. Examples of this "cookie cutter" effect are shown in Figure 8. Chemical attack has been eliminated by taping carrier perforations with a UV-release tape prior to BHF etching.

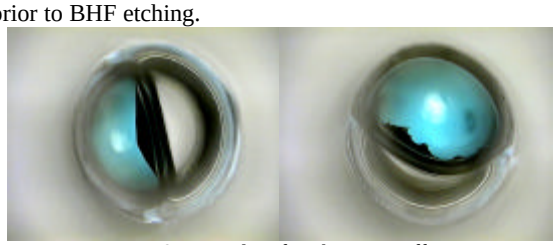

Figure 8: Examples of cookie cutter effect.

In addition, the fluorine-based plasma used for the SiON strip can wrap around the carrier and rapidly etch through the thermoplastic, exposing the frontside SiON to attack. Equipment modifications were made to minimize the exposure of the perforations to the plasma. An example of frontside etch is shown in Figure 9.

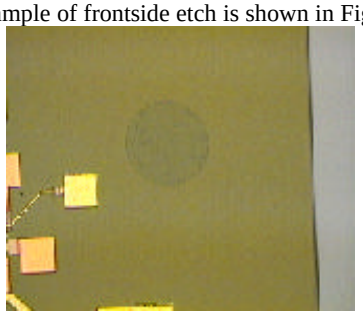

Figure 9: Frontside etch at carrier perforation

The last issue related to residue formation has been found to occur when chlorine-based, via etch gases react with exposed thermoplastic. The residue has been limited by the use of the older style carrier with the 6.6mm edge perforation exclusion zone. While this measure has been effective in eliminating most of this residue, it has increased dismount times.

NEW PROCESS IMPLEMENTATION

During the beginning of 2000, efforts were made to improve on capability, capacity and process simplification within the facility. The result of these efforts is a via process using a resist mask and Trikon's Omega® 201 ICP high-density plasma etch system. The ICP etch process implements an ~18µm thick layer of resist, patterned with a contact aligner, as the through via etch mask. With the cooled electrostatic chuck, resist reticulation during etching has been minimized [3].

The process conditions, as outlined in Table 3, have produced through wafer vias as shown in Figure 10.

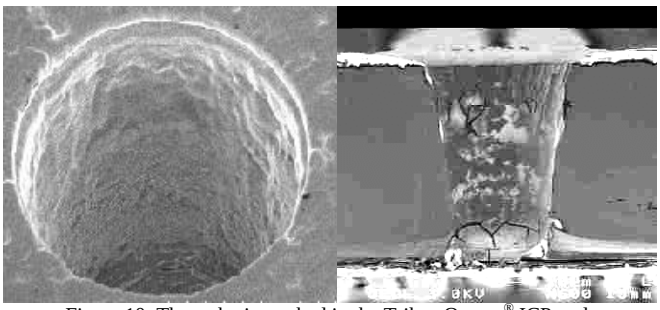

Figure 10: Through vias etched in the Trikon Omega® ICP tool.

TABLE 3
PROCESS COMPARISON

	RIE etcher	Trikon
Pressure	32 mTorr	40 mTorr
Gasses	48 sccm SiCl 16 sccm He	170 sccm Cl 10 sccm CF 9.5 Torr He BP
Power	80 W	ICP 900 W Bias 70 W
Highest Etch Rate	1µm/min	10µm/minute
Mask Material	5µm SiO_xN_y	>18µm Photo resist
Selectivity	~25:1	~20:1
Profile control	>90º	85°-90°
End pointing	No	Yes
Compatible with mini vias	No	Yes
Total via fabrication time	430 minutes	90 minutes

Many of the pitfalls encountered, while attempting mini vias with the standard process, were addressed using a resist mask and the Trikon ICP etch tool. First, the new process removed run out resulting from the stress induced by SiON deposition. It reduced the etch bias between the via mask and the final via dimension. Via dimensions from mask to frontside contact increased by an average of 2µm during lithography and GaAs dry etch. As well, the via profile out of the Trikon is positively sloped rather that re-entrant. As shown in Figure 11 and Figure 12, alignment is significantly improved, thus eliminating frontside metal shorting.

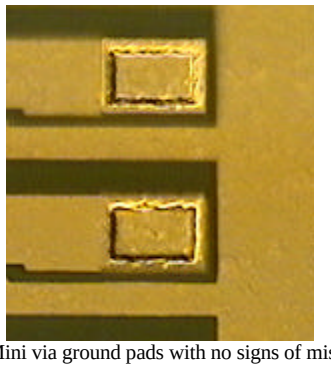

Figure 11: Mini via ground pads with no signs of misalignment.

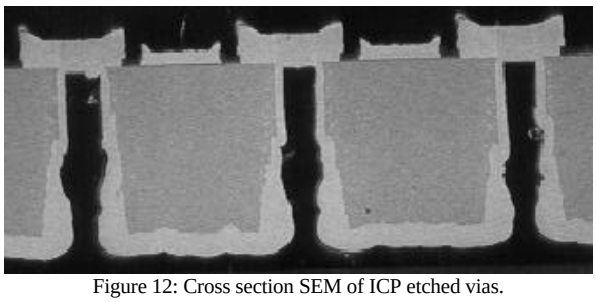

Figure 12: Cross section SEM of ICP etched vias.

IMPROVED MANUFACTURABILITY

In addition to the process capability improvements resulting from the Trikon Omega®, the added benefits of minimizing process steps and elimination of process bottlenecks resulted in the reduction of cycle times. When comparing via formation and etch process segments of the full SVia flow, the standard hard mask process has 22 steps with a theoretical cycle time of 430 minutes. With the resist-based process, the number of steps within this segment was reduced by 10 with a total theoretical cycle time of 92 minutes. In the conversion of processes, the two largest process bottlenecks, the SiON deposition and the RIE through via etch, were eliminated.

CONCLUSIONS

Nortel Networks' GaAs wafer backside manufacturing has been improved with new bonding, cleaning and via formation processes. Thermoplastic adhesives and improved chemical processes have improved thinning yield of FPHBT product circuits. A new resist-based process using a Trikon Omega® 201 ICP etch system has not only reduced cycle time by eliminating process steps, but has provided new capabilities, in particular, the realization of mini vias in 50µm-thick GaAs wafers. To our knowledge, the backside via etch rate established for this process is the fastest via etch rate achieved on any commercially available etch tool [4].

ACKNOWLEDGEMENTS

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ACRONYMS

BHF	Buffered HF
ESC	Electrostatic Chuck
FPHBT	Full Power HBT
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
HMDS	Hexamethyldisilazane
ICP	Inductively Coupled Plasma
MESFET	Metal Semi-conductor Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapour Deposition
RIE	Reactive Ion Etch
RF	Radio Frequency
Sccm	Standard Cubic Centimeter per minute
SEM	Scanning Electron Microscope
SiON	Silicon OxyNitride
SVia	Substrate Via
UV	Ultraviolet

TRADEMARKS