Characterization of a Manufacturable High Rate GaAs Via Etch Process

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Abstract

We report a high rate GaAs etch process for the formation of backside vias using a BCl_3 / Cl_2 chemistry in an inductively coupled plasma (ICP). Through a combination of process and hardware development a maximum GaAs etch rate of 6.9 um/min was achieved. The effect of a number of process parameters on GaAs etch rate was explored through the use of designed experiments. These experiments were centered around a 6.1 um/min process and examined the effect of

- **Pressure**
- **Process Gas Composition**
- **Substrate Bias Power and**
- **ICP Power**

on the GaAs etch rate and GaAs:Resist etch selectivity . The center point process was further verified in a manufacturing environment during an extended process marathon on 150 mm mounted and thinned substrates. Process results from the marathon are also reported.

INTRODUCTION

GaAs devices are used extensively in the wireless telecommunications industry, where the high electron mobility of GaAs makes it well suited for high frequency, low noise, high gain applications. Although it has excellent electrical properties, GaAs is a relatively poor thermal conductor, making it difficult to remove heat efficiently from power devices. A commonly used solution to this issue is the formation of vias from the wafer backside to the frontside circuitry. Such vias provide a good thermal path for heat removal as well as a low impedance ground for RF (radio frequency) devices.

Backside via formation is one of the final steps in the device fabrication. After completion of the frontside processing, the wafer is mounted face down on a carrier wafer and mechanically thinned to a thickness of approximately 100 microns. The back of the wafer is then patterned using photo-resist and the vias are plasma etched through the thinned substrate, stopping on the frontside metal. After resist removal the vias are metallized, typically by sputtering a gold seed layer followed by an electroless gold plating to act as the heat sink / ground connection.

For the via etch process, since it is necessary to etch ~100μm deep into the GaAs, a high etch rate is essential in order to obtain an acceptable wafer throughput. Also, a GaAs:resist selectivity of at least 10:1 is desirable, so that the required photo-resist thickness can be less than ~14μm, which is the maximum thickness typically achievable in a single spin. In order to ensure good metallization after etching, the via wall should have a sloped profile, with some control over the slope in order to accommodate the conflicting requirements of wall slope and reduced via dimensions.

In this work we describe the development of a production GaAs via process with an etch rate in excess of 6um/min and with a high and controllable GaAs:resist selectivity ratio. Using this in conjunction with a sloped resist profile, a variably sloped via can be obtained. In order to achieve the high etch rate, a high density Inductively Coupled Plasma source (ICP) is used, and independent control over the wafer bias provides selectivity control. The process is developed on 150mm diameter mechanical GaAs wafers using a DOE approach, and is verified in a 100 wafer production run using sapphire mounted, thinned wafers. The observation of needle-like features in the vias of the mounted/thinned wafers is discussed, and a correlation is made between the occurrence of these and the wafer type and process conditions.

EXPERIMENTAL

All wafers were etched in a Unaxis VLR 700 GaAs Via Etcher. This cluster tool uses an 2MHz ICP source to generate a high density plasma. Ion energy at the wafer is controlled by independently biasing the cathode at 13.56 MHz. Wafer temperature is regulated by electrostatically clamping the wafer to a liquid cooled cathode in conjunction with He backside cooling. Process endpoint experiments utilized

a Unaxis Spectraworks optical emission system (OES).

The substrates used in these experiments were 150 mm GaAs wafers patterned with a photoresist mask. The total exposed area of the test pattern was approximately 15% - a large portion of that area was due to a 3 mm photoresist edge bead removal required later in the process flow (exposed via area was 7%). Initial process development was performed on mechanical wafers while the final process verification utilized sapphire mounted, thinned slices which included a frontside metal etch stop.

All depth measurements were performed using a step profilometer. Mechanical GaAs samples were partially etched while the thinned, mounted samples were etched to completion.

RESULTS AND DISCUSSION

Plasma etch processes for GaAs typically utilize a chlorine-based chemistry. Though a Cl_2 plasma alone is sufficient to etch GaAs, additional reactants are often added to obtain a clean anisotropic etch. The goal of this work was to double the GaAs etch rate (from 3 um/min to 6 um/min) for a production qualified BCl_3 / Cl_2 process[1,2] without perturbing downstream manufacturability.

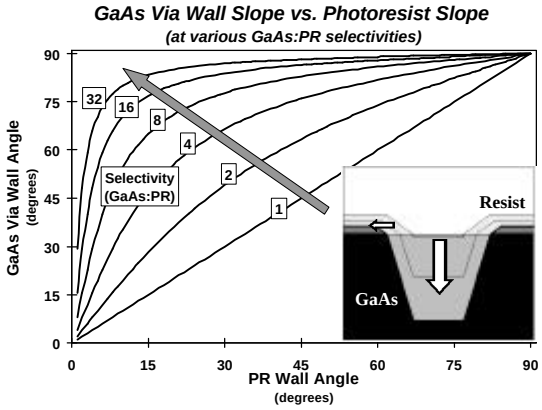

Figure 1. Expected GaAs via profile as a function of resist slope and GaAs:resist etch selectivity

While an anisotropic etch profile offers the best CD control, practically it is difficult to metallize. In order to lower the aspect ratio for ease of metallization, a sloped via profile is preferred. One approach to obtain a sloped via profile is through a combination of a sloped initial photoresist profile and controllable GaAs:Resist etch selectivity. This approach allows the initial resist profile to be "driven" into the via. ***Figure 1*** shows a model of the relationship between the initial resist profile and the expected GaAs via profile as a function of GaAs:Resist etch selectivity. The base line process prior to this work used this approach to achieve a sloped via. In order to minimize any impact on downstream operations (specifically metallization), it was important to maintain the baseline GaAs:Resist etch selectivity in order to maintain the baseline via profile.

Both hardware and process changes were required to achieve the 6 µm/min GaAs etch rate goal. Preliminary experiments showed that the GaAs rate increased with increased Cl_2 flows, requiring resizing of the MFCs. Further etch rate enhancements were achieved through modifications to the ICP source.

A designed experiment (DOE) was performed to map out the process space. While factorial experiments are a reliable way to map process responses, they quickly become cost prohibitive for a larger number of factors. Fractional factorial experiments are a convenient way to map factor responses, balancing time and material requirements with the quality of the calculated responses.

A four factor half fractional (2^{4-1}) design was chosen to explore the process window. This design explores the process space of 4 factors in only 11 experiments (8 + 3 centerpoint repeats) but is unable to resolve two factor interactions. If a two factor interaction is indicated in the statistical analysis, further experiments would be required to isolate the interaction. No significant

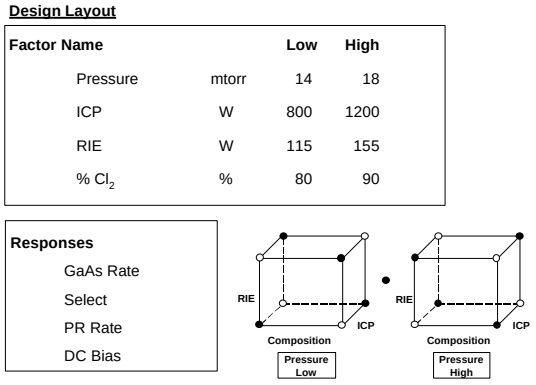

Figure 2. Summary of Designed Experiment. Range of factors explored and schematic of 2^{4-1} design

two factor interactions were found during the analysis of these designs.

The design examined the effects of four factors (pressure, ICP power, bias power, and reactant gas composition) on three responses (GaAs etch rate, resist etch rate, and GaAs:Resist etch selectivity). Process temperature, total gas flow, etch time and the hardware configuration were all held constant throughout the design. ***Figure 2*** shows the range of factors explored along with a schematic of the half fractional design. A post etch inspection of the wafers was performed using an optical microscope to check etch morphology. All cells of the DOE exhibited clean, smooth etched surfaces. Following inspection, the wafers were stripped and measured. ***Figure 3*** summarizes the DOE trends. The GaAs removal rate appears chemically driven – the GaAs etch rate increases with pressure, ICP power and increased Cl_2 fraction. Resist removal in a BCl_3 / Cl_2 chemistry appears physically driven – the resist etch rate increased solely with the RF bias power.

		Response		
Factor		GaAs Rate	Resist Rate	GaAs:Resist Selectivity
	↑ Pressure	↑		↑
	↑ ICP	↑		
	↑ RF Bias		↑	↓
	↑ % Cl_2	↑		

Figure 3. Response trends from Designed Experiment

The GaAs:Resist etch selectivity was found to be a function of both pressure and RF bias power. It is important to note that while the GaAs:Resist selectivity is a strong function RF bias power, the GaAs etch rate is bias power independent. Since the final via profile is a strong function of GaAs:Resist selectivity (***Figure 1***), the RF bias power can be used to adjust the final via profile independent of the GaAs etch rate. ***Figure 4*** maps the process space as a function of ICP power and pressure where the GaAs rate is greater than 6 µm/min and the GaAs:Resist selectivity is greater than 9.5:1.

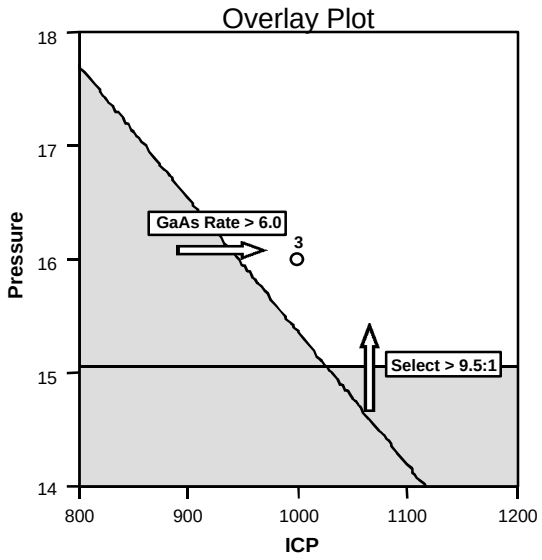

Figure 4. Process space as a function of process pressure and ICP power

In order to qualify the process for release to manufacturing, a 100 wafer etch marathon test was performed. The 100 wafer sample set was comprised of substrates from four different vendors. The wafers were metallized, mounted, thinned and patterned using identical processes. After patterning, the wafers were etched to full depth using the centerpoint process from the designed experiment. Etch end point was detected by monitoring the 417nm Ga line by OES. After every 10th mounted wafer was etched, a mechanical wafer was partially etched (10 minutes) to monitor etch rate and selectivity. (***Figure 5***) The mechanical etch monitors ranged

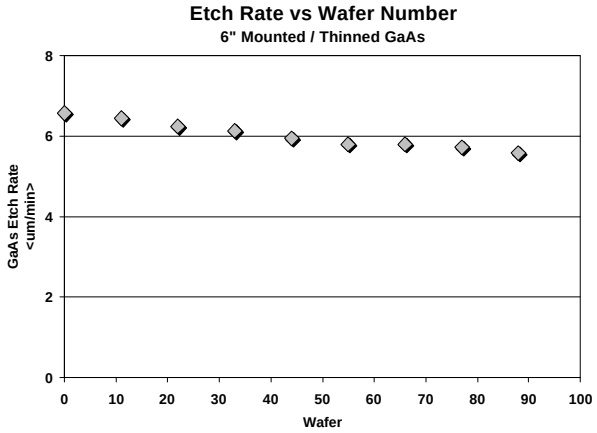

Figure 5. GaAs etch rate from 100 wafer process marathon. Etch rate measured on partially etched mechanical GaAs wafers

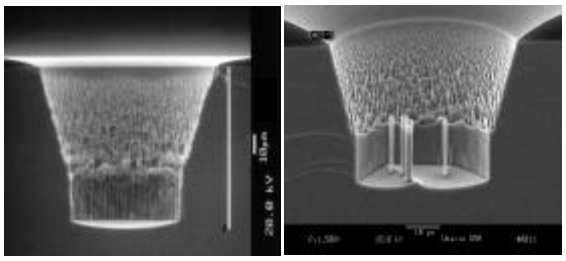

Figure 6. SEM cross section of via with and without grass formation. Note sloped profile

from 5.6 to 6.6 µm/min during the course of the process marathon.

A post etch inspection of the marathon wafers was performed using an optical microscope to check etch morphology. Sparse grass was present in a fraction of the vias on a number of wafers (***Figure 6***). The formation of grass during via etching has been previously reported in the literature by Nam et al.[3] In order to quantify the extent of grass formation, data was collected from 15 vias on each of 7 sites in a diagonal pattern on each wafer counted. Four wafers from each vendor representing a minimum of 3 boules per vendor were analyzed.

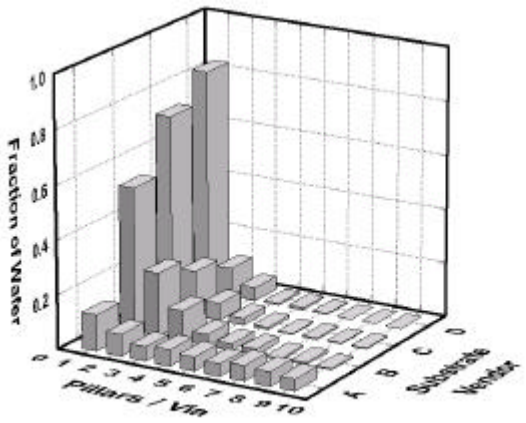

Figure 7. Pillar formation as a function of substrate supplier. Material D shows 80% pillar free vias. Material A shows 10% pillar free vias.

Each via was binned according the number of pillar-like grass structures present in the via. ***Figure 7*** shows the correlation between the material supplier and pillar formation. Material D exhibited an areal density of 0.51 pillars/mm^2 with 80% grass free vias, while material A had an areal density of 6.03 pillars/mm^2 with only 10% of the vias pillar free. Further reductions in pillar density were achieved through additional process development using the worst case material (Material A).

CONCLUSIONS

A 75% improvement in via etch throughput was achieved by a combination of process and hardware developments. The GaAs etch rate of a production proven 150 mm GaAs via etch process was doubled from 3 µm/min to 6 µm/min with minimal impact on downstream processes. Using a sloped resist mask, sloped via profiles are achieved through resist erosion at reduced (11:1) GaAs:Resist selectivities. Designed experiments show that the RF bias power can be used to control the final via profile independently of the GaAs etch rate. Sparse grass formation seen in some design cells was influenced by material supplier as well as process conditions. Etch endpoint detection has been demonstrated through monitoring the 417 nm Ga line by optical emission spectroscopy (OES).

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