Manufacturable GaAs High Power FET for W-CDMA Base Station

E. Mitani*, H. Takahashi, H.Haematsu, K. Inoue, K. Ebihara and J. Fukaya

Fujitsu Quantum Devices Ltd.
1000 Kamisukiawara, Syowa-chou, Nakakoma-gun, Yamanashi-ken 409-3883, Japan

*) Fujitsu Compound Semiconductor, Inc.
2355 Zanker Road, San Jose, CA 95131-1138
E-mail : emitani@fcsi.fujitsu.com , Phone : (408) 232-9610

Abstract

We have been developing high power GaAs based FET for W-CDMA base stations system. Our quasi enhancement-mode (E-mode) structure realizes both high efficiency and low distortion. Through the sophisticated process technology and circuit design, the device shows very good repeatability and reliability. The actual production data of 150W FET shows the standard deviation of pinch-off voltage is 46 mV and standard deviation of output power is 0.52 dB. The high temperature operation test result shows very high reliability with a MTTF of ~1 x 10^6 hours for a channel temperature of 175 °C.

INTRODUCTION

The development of high output power devices for W-CDMA base stations has been the purpose of our work in recent years.[1)~3)] Table 1 shows the standard performance of our devices. A device capable of 300W has been successfully demonstrated and mass-production is under way for the 240W devices. All devices consist of four GaAs FET chips, fabricated with our high efficiency and low distortion technology, combined in a push-pull configuration.

This paper describes the key points to obtain high performance in such a high power FET. It also demonstrates good repeatability and high reliability under actual mass-production, confirmed by data obtained in high temperature operation test.

Table 1
Typical electric characteristics of high power GaAs FETs for W-CDMA base station systems.
f = 2.17 GHz, V_{DS} = 12 V

Device	P_{out} (dBm)	GL (dB)	Status
80W FET	49.0	11	Mass-production
150W FET[1)]	51.8	12	Mass-production
240W FET[2)]	53.8	11.5	Mass-production
300W FET[3)]	54.8	11	Under development

CHIP STRUCTURE

A GaAs epi-base MESFET structure was adopted for the high power FET. The chip structure consists of a Si doped GaAs channel layer, AlGaAs schottky layer and GaAs cap layer with WSi/Au T-shaped gate and Au/Ge/Ni/Au alloyed ohmic contacts. All active areas are covered with SiN passivation.

To realize high power and high linearity GaAs FET chips for W-CDMA application, the 2 keys points are:

1) High transconductance (g_m) : Based on Volterra series analysis, the 3rd order intermodulation distortion (IM3) ratio was found to be directly related to $g_{m.}$ Increasing g_m is a very effective method to get better linearity.[4)] Using a device simulator, we concluded a high doped, thin channel quasi enhancement mode FET is the best structure to improve both the power-added-efficiency (PAE) and linearity.

2) Low thermal resistance (R_{th}) : The thermal design is a very critical issue for such a high power device. With the limitation of a practical chip width, the unit gate width (W_{gu}) and the gate-to-gate length (L_{gg}) were optimized considering the trade-off relationship between RF gain characteristics and thermal resistance. In addition, a plated-heat-sink (PHS) structure is adopted to optimize thermal transfer. The GaAs wafer is thinned to 28 um and the gold on backside is plated up to 30 um.

Fig.1 is a photograph of the 60W output chip used in the 240W device. Each chip consists of 14 cells with 16 gate fingers each. W_{gu} is 870 um, so the total gate width (W_{gt}) is 195 mm. The chip size is 4.0 x 1.4 mm^2.

Copyright 2002 GaAsMANTECH, Inc.

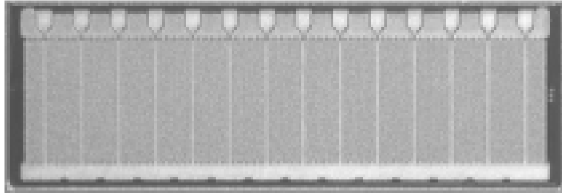


Figure 1 Photograph of 60W output chip

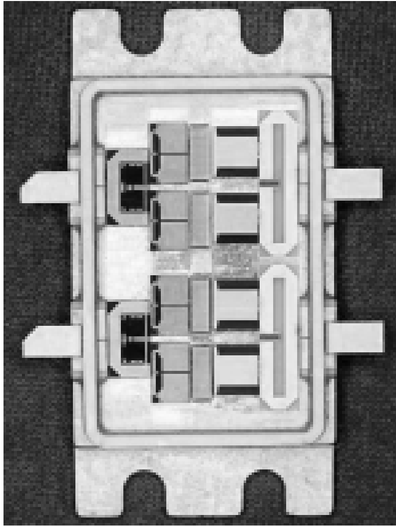


Figure 2 Top view of 240W push-pull FET

CIRCUIT DESIGN AND POWER PERFORMANCE

Fig.2 shows a photograph of the 240W push-pull power FET. The package size is 34.0 x 17.4 mm^2. A pair of 60W output power chips is combined with in-phase divider and combiner and two sets of the combined chips are assembled in the package to be used in a push-pull configuration. The optimum impedance of each chip port was estimated from load-pull measurement.

Fig.3 shows the measured output power and power-added efficiency (PAE) of the 240W push-pull FET at 2.14 GHz. A saturation power of 53.8 dBm (240 W) was achieved with a linear gain of 11.5 dB and a power-added efficiency of 54 %.

Fig.4 shows the measured adjacent channel leakage power ratio (ACPR) measured by using W-CDMA modulation signal. It was obtained an ACPR level of –36 dBc with associated PAE of 24 %.

REPEATABILITY

Fig.5 (a)~(d) show the distribution data of 150W devices in mass-production. These data come from random sampling from our shipping data of actual products from January to November 2001. Total device number is about 2400 from 50 wafers in various lots and periods.

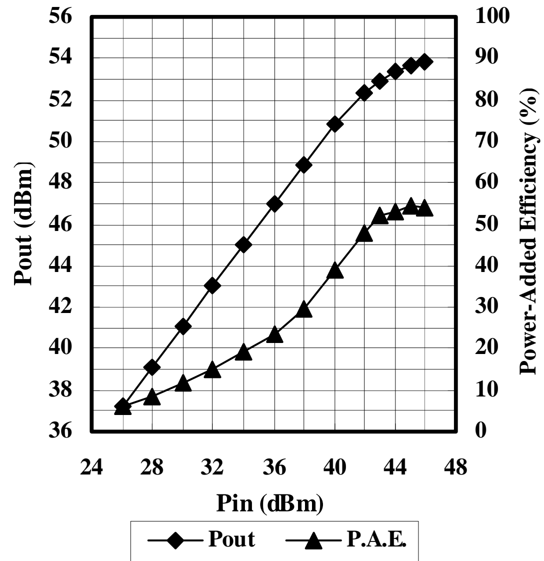


Figure 3 Output power and power-added efficiency versus input power. f=2.14 GHz, V_{DS}=12 V, I_{DS}(DC)=6.0 A.

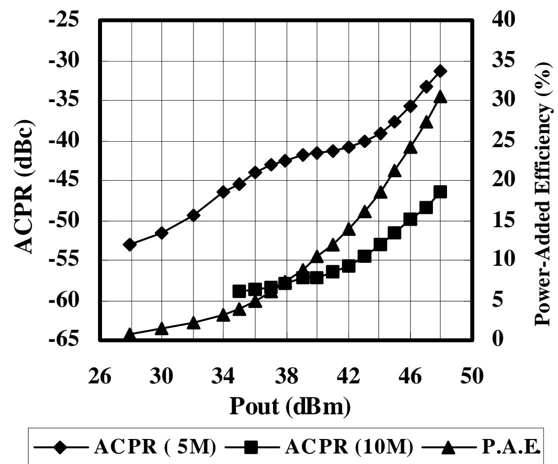
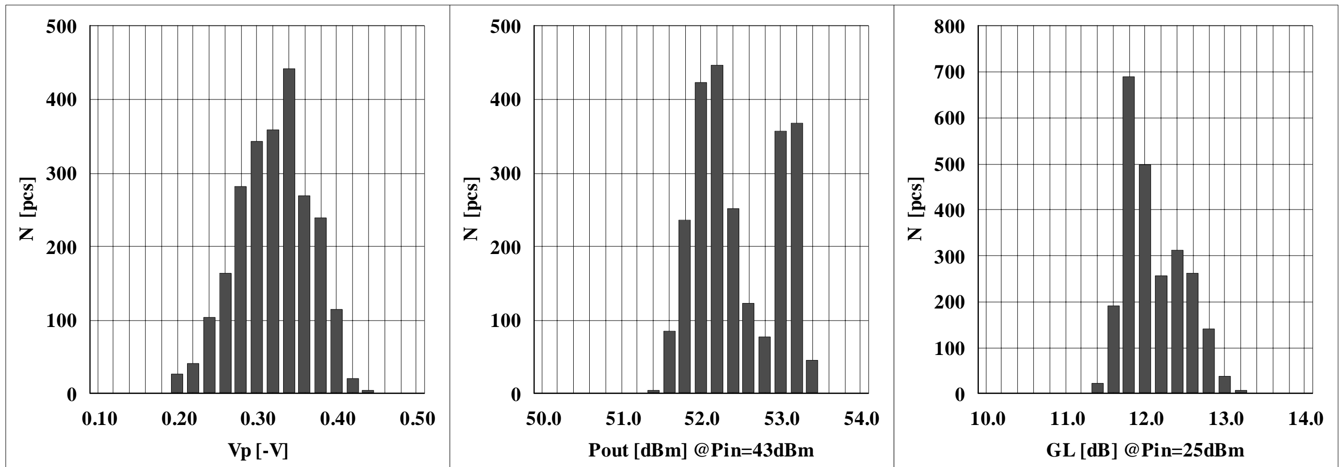


Figure 4 ACPR and power-added efficiency versus output power. f=2.14 GHz, V_{DS}=12 V, I_{DS}(DC)=6.0 A.

Fig.5 (a) shows the distribution of pinch-off voltage (V_p). The average value is –0.31 V and the standard deviation is 46 mV. This small distribution of V_p is the result of precise control of the gate process through selective dry etching of the GaAs cap layer and gate metal formation. In addition, monitoring epi wafers using the sheet resistance measurement and C-V measurement proved to be very effective.

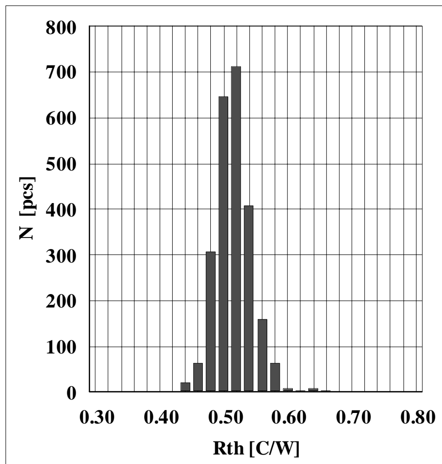
Fig.5 (b) and (c) show the distribution of output power (P_{out}) and linear gain (GL) respectively. The average P_{out} is



(a) Pinch-off voltage @V_{DS} = 5 V

(b) Output power @V_{DS} = 12 V, P_{in} = 43 dBm, f = 2.17GHz

(c) Linear gain @V_{DS} = 12 V, P_{in} = 25 dBm, f = 2.17GHz



(d) Thermal resistance

Figure 5 (a) ~ (d) Distribution data of 150W FETs --- Sampling from shipment test results

52.4 dBm and standard deviation is 0.52 dBm. The average GL is 12.0 dB and standard deviation is 0.37 dB. This small distribution is the result of both the good uniformity of the FET chips and optimized circuit design.

Fig.5(d) shows the distribution of thermal resistance (R_{th}), which was measured by delta VGS method. The average value is 0.51 °C/W and standard deviation is 0.03 °C/W. As a result of the optimized thermal design, the thermal resistance is low and very uniform.

These data show a very good repeatability for the FETs. Such good repeatability not only leads to high yield in our production, but also results in lower cost for the base station amplifier manufacturers.

RELIABILITY

The devices used for infrastructure applications such as base station system are also required to present a high reliability. A high temperature operation test was performed to define mean time to failure (MTTF) of the device. The test was conducted with 10W class chips. The channel temperature (T_{ch}) was set to 220 °C. The failure criteria was defined as a reduction in power or gain of >0.5 dB and >0.8

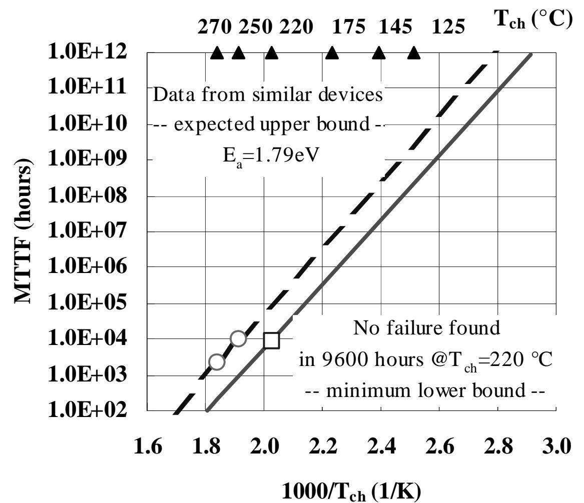


Figure 6 Estimated MTTF versus T_{ch}

Solid line : Lower-limit MTTF for high power FET

Dashed line : MTTF for similar GaAs FET

Copyright 2002 GaAsMANTECH, Inc.

dB respectively. The test result showed no failure up to 9600 hours.

To estimate MTTF of the actual operating channel temperature, we assumed the activation energy (E_a) is equal to 1.79 eV, which was extracted from the test conducted to GaAs FETs made by a similar process. Fig.6 shows the Arrhenius plot of the estimated MTTF. The dashed line shows the test results of the similar devices and their extrapolated line. This means the expected upper bound of MTTF. The solid line shows the estimated MTTF, assumed MTTF at T_{ch} = 220 °C as 9600 hours, which is the lower bound. The estimated MTTF is longer than at least 6.6 x 10^5 hours at T_{ch} = 175 °C. The wafer process and assembly lines for these high power FETs are basically the same as for space application products. Such space qualified technologies work well for the high reliability of these high power FETs.

CONCLUSIONS

We have successfully developed GaAs high power FETs for W-CDMA base station systems. Using a quasi enhancement mode FET, we could achieve both high efficiency and low distortion. The optimized thermal design resulted in a high power device. We have started mass-production of up to 240W FETs. Through the sophisticated process technology and circuit design, the device shows very good repeatability and reliability. The actual production data of the 150W FETs show the standard deviation of pinch-off voltage is 46 mV and standard deviation of output power is 0.52 dB. The high temperature operation test result shows very high reliability with a MTTF of ~1 x 10^6 hours for a channel temperature of 175 °C. These advantages in performance, repeatability and reliability indicate our GaAs high power FETs are suitable for use in W-CDMA base station systems.

ACKNOWLEDGEMENTS

The authors would like to thank T. Iida, F. Yamaki, Y. Nakasha and M. Suzuki for their helpful discussions and encouragement for this work.

REFERENCES

[1] Y.Tateno, H.Takahashi, T.Igarashi and J.Fukaya, "A 150W E-mode GaAs Power FET with 35% PAE for W-CDMA Base Station", 1999 IEEE MTT-S Digest, pp.1087 – 1090.

[2] K.Inoue, K.Ebihara, H.Haematsu, T.Igarashi, H.Takahashi and J.Fukaya, "A 240W Push-pull GaAs Power FET for W-CDMA Base Stations", 2000 IEEE MTT-S Digest, pp.1719 – 1722.

[3] K.Ebihara, K.Inoue, H.Haematsu, F.Yamaki, H.Takahashi and J.Fukaya, "An Ultra Broad Band 300W GaAs Power FET for W-CDMA Base Stations", 2001 IEEE MTT-S Digest, pp.649 – 652.

[4] Y.Nakasha, M.Nagahara, Y.Tateno, H.Takahashi, T.Igarashi, K.Joshin, J.Fukaya and M.Takikawa, "A Low-Distortion and High-Efficiency E-mode GaAs Power FET Based on an New Method to Improve Linearity Focused on gm Value", 1999 IEDM Technical Digest, pp.405 – 408.

Copyright 2002 GaAsMANTECH, Inc.