Manufacturable 0.15 um PHEMT Process for High Volume and Low Cost on 6" GaAs Substrates : The First 0.15 μm PHEMT 6"GaAs Foundry Fab

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Abstract

A successful development of very high performance and reliable 0.15 um power and low noise PHEMTs on 6 inch GaAs substrate is reported for the first time. Our 0.15 μm PHEMT demonstrated state of the art power performance at 32 GHz, an output power of 390 mW with PAE of 32 % was achieved from unit cell of 8x75 μm. The 0.15 μm low noise PHEMT shows very good noise performance NF of 0.75 dB at 20 GHz. Excellent reliability of our power and low noise PHEMTs was achieved for more then 3000 hours at channel temperature exceeding 235°C. Yield exceeding 80 % was demonstrated for 9200 devices with 1.2 mm gate width across a 6-Inch GaAs wafer. These results indicate that the 0.15 μm PHEMT technology is ready for high volume production with low cost at Win Semiconductors.

Introduction

The demand for millimeter wave GaAs products has increased such that the technology is expanding beyond niche markets and is entering the commodity markets. The ultimate acceptance of GaAs in commercial applications, however, depends upon its ability of providing the lowest cost solution compared to other technologies. As an example, A 77 GHz automotive radar system for car collision avoidance and intelligent cruise control has recently gained interest because of its huge market potential and it will be with GaAs millimeter wave technology. The questions of the optimum technology leading to both low cost and high performance have not yet been answered. In order to address the needs for both high performance and low manufacturing cost, for the first time, an e-beam 0.15 um PHEMT process has been developed on six inch GaAs substrates with high yield and reproducibility for production.

Device and MMIC Fabrication

The starting material is a GaInAs/AlGaAs PHEMT grown on 6-inch GaAs substrate. Mesa, TaN resistor 50 Ohm/sqr or 25 Ohm/sqr, 0.15 um Y-Gate defined with e-beam, selective gate recess, Au **based air-bridge**, dry etching technology for slot via (4 or 2 mil thick substrate technology) were used to fabricate the MMICs. The backside process including thinning, polishing, and wafer demounting still remain a challenges for 6 inch GaAs substrate. For power applications, it is better for large FETs to have a slot rectangular via under each source pad for grounding. This will help to improve the thermal dissipation, thus the MMIC reliability, as shown in fig.1.

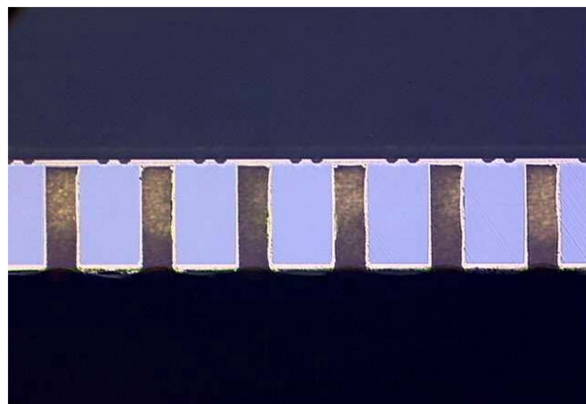

Fig.1: Typical via holes cross section of multi-finger Power PHEMT thinned to 4 mil.

Test structure was laid out on PCM designed to monitor the via hole continuity and consist of 23 via holes in series. The via holes process

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yield was greater than 99 % across 6-inch GaAs wafer with very high reproducibility.

Device Performances and Characteristics

WIN 0.15 um DR PHEMTs consist of double side doped with double recess to achieve high current density with high breakdown, as shown in fig.2. An extrinsic Transconductance of 500 mS/mm with maximum drain current of 660 mA/mm and breakdown of 10 V is routinely achieved. At V_{DS}= 1.5 V, a mean ft of 90 GHz with standard deviation of 4 GHz is typically achieved on 6 inch-GaAs wafers.

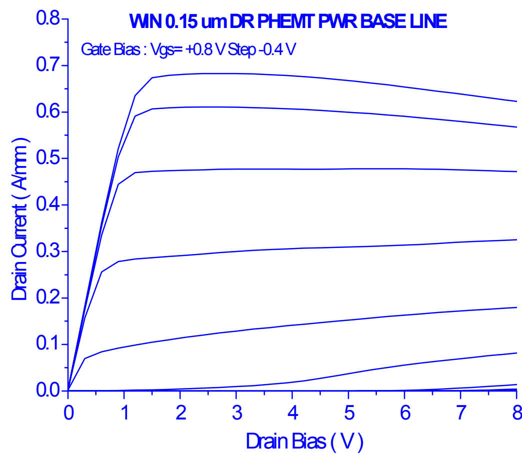


Fig.2 : Typical I-V Characteristics of WIN 0.15 um Power PHEMT

A load pull power measurement of unit cell (8x75µm) with 0.15 µm gate length demonstrate at 32 GHz a P_{sat} of 390 mW with maximum PAE of 32 % and linear gain of 9.8dB, as showed in fig.3. A high P_{1dB} of 500 mW/mm with PAE of 28 % is achieved at peak-gm (I_{DS}=200 mA). Our 0.15 um double recess power PHEMT process is very suitable for HPA at Ka-band with high linearity.

Figure 4 shows the tight distribution of PCM DC characteristics of 50 wafers from different lots and different Epi batches. The excellent yield and reproducibility are mainly related to well controlled gate recess, giving a ΔVp less then 100 mV across 6" wafer, well defined e-beam lithography and state of the art Epi calibration. Figure 5 shows a yield estimation of 76 % for large devices (8x150 um) across 6-inch GaAs wafer for 9160 devices. The drain current at fixed gate bias of -0.4 V was 325 mA/mm with Std of 25 mA/mm. These results show that WIN 0.15 um PHEMT process has very high capability for production of high volume MMIC. This allows our customers to have very high ability to design any MMIC to meet given performance specifications with high accuracy and yield

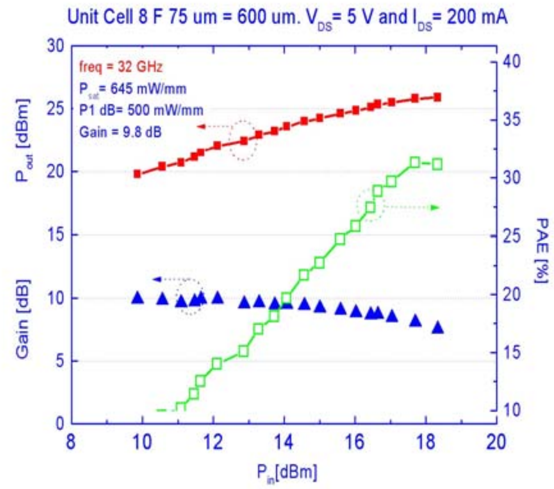
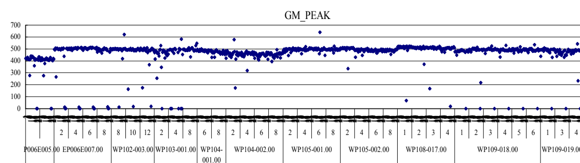


Fig.3: Measured Gain, Pout and PAE for 8x75 um 015 un PWR PHEMT at 32 GHz.



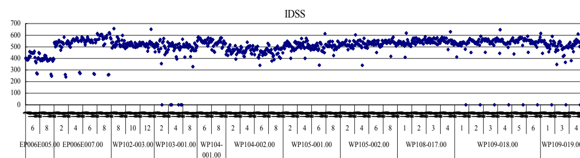


Fig.4: SPC control chart for g_m, I_{DSS} and V_p of WIN 0.15 um PWR PHEMT for 50 wafers.

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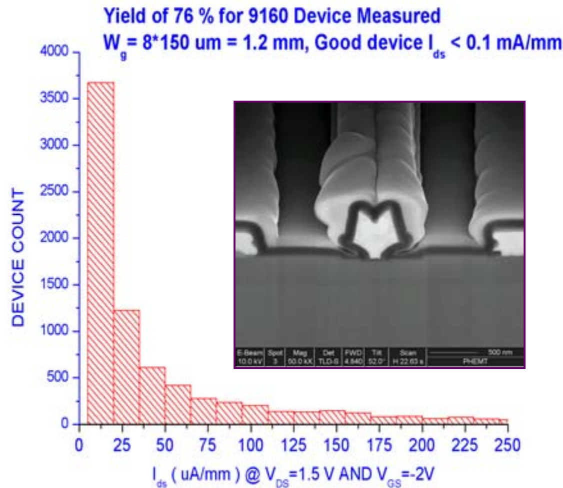

Fig.5: Yield estimation of WIN 0.15 um PWR PHEMT wafer. A cross-section of WIN 0.15 um Y-Gate showing excellent conformal coating of the SiN.

The WIN 0.15um LN PHEMT consists of single side doped structure with single recess. A peak-gm of 580 mS/mm at V_{GS}= 0 V and Gate-Drain breakdown of 9 V with an f_t of 100 GHz and an f_{max} of 160 GHz is routinely achieved on 6“ GaAs substrate. The WIN 0.15 um LN PHEMT process also shows high reproducibility and uniformity wafer to wafer and lot to lot with DC and RF yield exceeding 90 %. The devices showed an excellent noise figure of 0.75 dB and associated gain of 9 dB at 18 GHz, as shown in fig.6. Thus, WIN 0.15 um LN PHEMT is very suitable for Low Noise amplifier at millimeter wave.

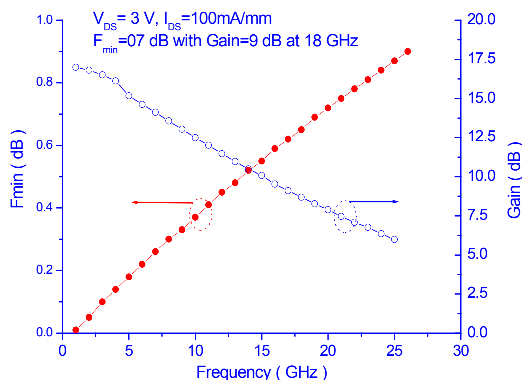

Fig.6 : Noise performance of WIN 0.15 um LN PHEMT

Device Reliability

Even the highest performance device is of little use if the reliability fails to meet requirements. DC life test was carried at different temperatures on 20-22 devices of 0.15 um Power and Low Noise PHEMT with gate width of 2x75 um.

The power PHEMT devices were stressed at V_{DS}= 5 V and 30 % Idsmax, corresponding to DC dissipated power of 1 Watt/mm. The devices were stressed at different channel temperatures of 275 °C, 260 °C and 235 °C. Our Criterion is 20 % degradation in maximum drain current defined at V_{DS}=1.5 V and V_{GS}= + 0.6 V. The figure shows the robustness of our WIN 0.15 um power process. We have only 10% degradation in I_{DSmax} after 3500 hours bias stress at T_{ch} of 275 °C, as shown in fig.7. After 3000 hours at channel temperature of 235 °C the devices were very stable.

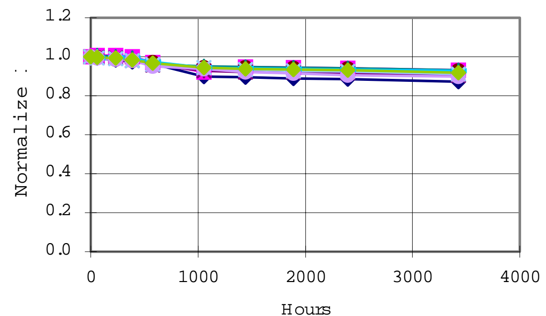

Fig. 7: DC life test of WIN 0.15 um Power PHEMT at VDS= 5 , I_{DS}= 200 mA/mm and T_{ch}=275 °C.

RF life tested for unit cell 2x75 um was carried at 250 °C and 275 °C channel temperature and under 2 dB compression at 20 GHz with V_{DS}= 5.5 V. The devices shows only 0.3 dB degradation for 275 °C group and virtually no degradation for 250 °C group up to 950 hours, as shown in fig.8. The devices got a RF burn-in at 175°C for 300 hours under 2 dB compression and V_{DS}= 5 V and shows no significant degradation. These results confirm well the DC bias stress. The WIN 0.15 um DR PHEMT

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process is highly reliable and suitable for production high volume low cost HPA at millimeter wave.

Tch= 275 C

Fig. 8: RF life test at 20 GHz of WIN 0.15 um Power PHEMT at V_{DS}= 5 V.

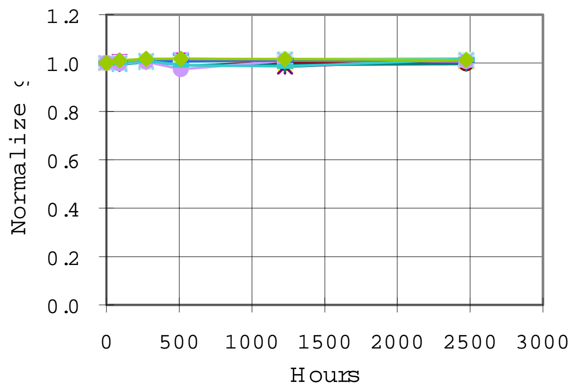

Fig. 9: DC life test of WIN 0.15 um Low Noise PHEMT at V_{DS}= 3V and T_{ch}=240 °C.

Low Noise PHEMT the devices were stressed at V_{DS}= 3 V, gate bias corresponding to peak-gm and T_{ch} of 230 °C, 200 °C and 185 °C (DC power dissipated is 830 mW/mm). Our Criterion is 20% degradation in peak-g_m. The figure shows the robustness of our WIN 0.15 um Low Noise process. The devices were very stable without any degradation at channel temperature of 230 °C at 3 V drain bias for 2500 hours, as shown in fig.9. These results confirm the excellent passivation process of WIN 0.15um Low noise and Power PHEMT.

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Applications of WIN 0.15 μm Power and Low Noise PHEMT

WIN 0.15 um LN PHEMT makes it very suitable for low noise amplifiers to V-band for radio links, LMDS and also digital radio. The future real big market for WIN 0.15 um LN PHEMT is car avoidance radar at 77 GHz. With GaAs PHEMT, all functions can be realized in one single chip, including the transmitter (15-30 mW), the receiver (NF=7-8 dB) and the VCO. With WIN 0.15 um LN PHEMT on 6-inch GaAs substrate the prize of all set chips will be much lower then the predicted production prize target of 100 US$. In addition, the 0.15 um PHEMT low noise process seems to be a more logical choice for 40G Fiber-Optic Communications. The high f_T and breakdown of WIN 0.15 um LN PHEMT makes it very suitable for trans-impedance amplifier (TIAs) for receivers and modulator which require high voltage drive level (8 V peak-peak). Our customers for OC-768 have already qualified this technology. Knowing that the receiver function needs only 2x1 mm^2, this will make TIAs cost for 40 G less then 8 US$ for volume production.

The recent growth in the point to point and point to multipoint radio markets also Sat-TV has generated the requirement for high power amplifier at Ka-Band. WIN 0.15 um Power PHEMT is very suitable for Sat-TV and LMDS with cost advantage. Usually, 1 Watt at 30 GHz is achieved within 2x1.5 mm^2 by our technology. Thus, 1 Watt at Ka-Band can meet the production target prize for high volume of 10 US$ amplifier. Our customers also qualified this technology for LMDS and also OC-768 driver laser.

In conclusion, we have demonstrated 6” GaAs wafer with 0.15 um PHEMT technology. High throughput e-beam lithography technology has been used for uniformity, high yield and reproducibility. Excellent reliability has also been demonstrated. This is the first successful demonstration of 0.15 um PHEMT technology for foundry service on 6” GaAs substrates

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