Silicon Nitride MIM Capacitor Reliability for Multiple Dielectric Thicknesses

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***Abstract*- A single GaAs MMIC fabrication flow produces three different types of silicon nitride capacitors, with 50 nm, 200 nm, and 250 nm nominal dielectric thickness. Ramped voltage data indicates that all three types are reliable. The results are compared to predictions of the linear field and Frenkel-Poole conduction models for capacitor lifetime at fixed voltages.**

INTRODUCTION

Typical GaAs MMIC processes include multiple metal interconnect layers and multiple dielectric depositions. MMIC processes with multiple options for capacitor dielectric thickness offer significant advantages. A 50 nm silicon nitride dielectric can be used for bypass or blocking applications, where high capacitance density is a priority. A 200 nm or a 250 nm dielectric can be used for microwave tuning elements, where capacitance precision is a priority, or where higher voltage operation is required. In this work, we demonstrate the use of different combinations of interconnect metals and dielectrics to construct reliable capacitors.

Ramped voltage testing provides a rapid and efficient means of assessing reliability and determining appropriate application voltage ranges for each type of capacitor. Ramped stresses can be readily applied using automated test equipment, in a predictable, short time period. Available theories provide a means of predicting operating lifetimes from ramped voltage data. Fixed voltage tests are more representative of actual operating conditions; however, they are time consuming and not well suited to automated wafer probe environments.

In this work, we compare ramped voltage performance of three capacitor types, with 50 nm, 200 nm, and 250 nm nominal dielectric thickness, at both positive and negative polarities. Additionally, we compare ramped voltage and fixed voltage results for 50 nm capacitors. To monitor the quality and reliability of capacitors, we regularly fabricate capacitor test pattern lots. Data and analysis below is for a representative process monitor lot.

FABRICATION FLOW

The fabrication process combines high performance dual-recess 0.25 µm pHEMT devices with high density interconnect metalization. This process is similar, but not identical to, that described in [1].

This work concerns three capacitor types, constructed using the layers described in Table 1. For the purposes of this paper, we name the three capacitor types "CT50," "CT200," and "CT250," based on the nominal dielectric thickness.

TABLE 1
CAPACITOR CONSTRUCTION

capacitor type	bottom plate metal	dielectric	top plate metal
CT50	Metal0	Nitride1	MIM
CT200	MIM	Nitride2	Metal1
CT250	Metal0	Nitride1 + Nitride2	Metal1

The Metal0 and "MIM" metal layers are deposited by e-beam evaporation. They are layered metal stacks composed primarily of gold. The Metal1 layer is fabricated using a sputter-deposited field metal followed by gold electroplate. The 50 nm Nitride1 and 200 nm Nitride2 layers are deposited by PECVD.

RAMPED VOLTAGE TESTING

The capacitor test array consists of a variety of capacitor structures designed for use as a regular process monitor. All capacitors tested for this study have a square top plate, 100 µm x 100 µm. Four voltage ramps were applied: +4.0 V/s, -4.0 V/s, +0.4 V/s, and -0.4 V/s. All measurements were performed at room temperature. The automated probe tested a cross pattern, in the horizontal and vertical directions, across the center of the wafer. The pattern included samples of each capacitor type at each ramp condition, a total of 39 x 3 x 4 = 468 capacitors per wafer. The ramp is approximated by a series of 0.25 V steps, and

failure is detected when the capacitor leakage current exceeds 10 mA.

Table 2 lists the median and standard deviation for ramp failure voltages on the five process monitor wafers. There were no deliberate differences between the wafers, and the variations in measured failure voltage are due to natural variation in the fabrication processes. Note that the negative polarity failure voltages are somewhat higher than the positive polarity voltages. For CT250 at the negative polarity, some wafers exceeded the 200 V limit of the test equipment. None of the samples represented in Table 2 failed at less than 80% of the wafer median, so for the purposes of analysis we will treat this sample as approximately defect-free, or "intrinsic."

TABLE 2
MEDIAN AND STANDARD DEVIATION OF FAILURE VOLTAGE USING 4.0 V/s RAMP, V

	Polarity:	+	+	+	−	−	−
Wafer	Type:	CT50	CT200	CT250	CT50	CT200	CT250
A	Median	38.5	126.9	160.9	40.0	150.4	190.7
B	Median	37.5	124.1	155.7	39.3	162.2	200*
C	Median	37.5	127.9	167.2	39.0	153.2	192.5
D	Median	39.0	136.1	174.7	40.5	147.7	191.5
E	Median	38.3	157.9	197.0	39.8	166.2	200*
A	Std. Dev.	0.3	7.6	13.6	0.3	2.5	2.1
B	Std. Dev.	0.2	7.3	8.7	0.2	0.9	0.9
C	Std. Dev.	0.3	9.6	11.7	0.3	1.6	1.8
D	Std. Dev.	0.3	1.6	1.9	0.2	2.1	1.2
E	Std. Dev.	0.3	0.8	2.6	0.3	0.9	0.2

* Test equipment limited to 200 V.

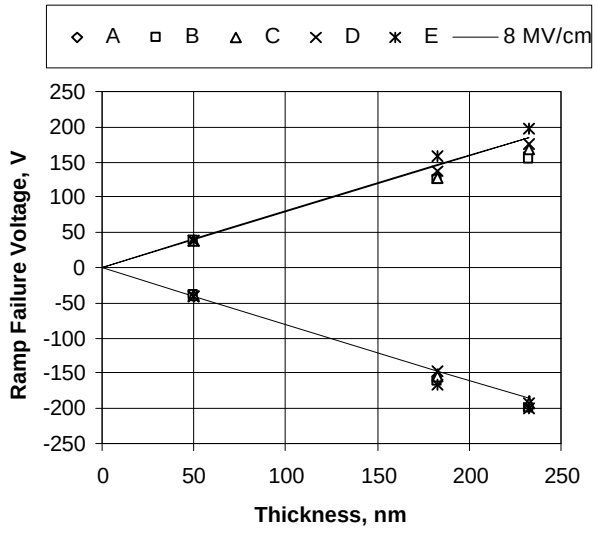


Fig. 1: Median failure voltages for 4.0 V/s. Both polarities are displayed, and a line drawn at 8 MV/cm is included for reference.

Figure 1 displays the median failure voltages as a function of nitride thickness for 4.0 V/s, including both polarities. Note that CT200 and CT250 dielectric thickness values are offset from nominal; the sputtering process used to deposit the field metal for the Metal1 top plate removes approximately 17.5 nm from the Nitride2 dielectric. The values lie roughly along a line at 8 MV/cm; however, negative polarity values are somewhat greater in magnitude, and positive polarity values somewhat less.

Positive bias to top plate results in lower failure voltages. This polarity dependence in ramped voltage performance is not explained by the available theories. Polarity dependence may be due to the inherent asymmetry in MIM cap construction: the top plate is smaller than the bottom plate, and higher fields will exist at the top plate edges. The basic wear-out mechanism for MIM capacitors is presumed to be the accumulation of negative, trapped charge in the dielectric. Under positive bias, this results in an increase in field strength at the top plate and a corresponding reduction in field strength at the bottom plate. The reverse is true for negative bias: the field increases at the bottom plate and decreases at the top plate. Thus, the critical field is reached first at the top plate under positive bias and at the bottom plate under negative bias. Since the bottom plate extends out from the top plate by many multiples of the dielectric thickness, it has no high field concentration point, and can apparently withstand higher levels of applied voltage under negative bias.

LIFETIME PREDICTIONS USING RAMPED VOLTAGE DATA

The widely used linear field model [2-3] provides a method for projecting capacitor lifetime under operating conditions based on ramped voltage data. According to this model, the time to failure *t(F)* is given by:

$$t(F) = t(0)\exp[\gamma(E_F - E_A)] \qquad (1)$$

where

$$t(0) = \frac{\Delta t}{1-\exp(-\gamma\Delta E)}, \qquad (2)$$

Δt is the ramp step time, ΔE is the ramp field step, E_F is the field at failure, and E_A is the field at the application voltage.

The acceleration parameter γ is obtained from the median failure voltages at two different ramp rates:

$$\gamma = \frac{\ln\left(\frac{R_1}{R_2}\right)}{E_1 - E_2} \qquad (3)$$

where R_1 is the fast ramp rate, R_2 the slow ramp rate, E_1 the field at fast ramp failure, and E_2 the field at slow ramp failure.

Table 3 lists values of γ for each capacitor type and polarity, based on the median ramp failure voltages. These values show some wafer to wafer variation. This is due to a combination of inherent process fluctuations and statistical variations caused by the small sample size. When predicting device lifetimes, we prefer to use average values based on larger sample sets. The lot average values of γ for the different capacitor types are all within about 10% of 40 nm/V.

TABLE 3
ACCELERATION FACTOR γ, nm/V

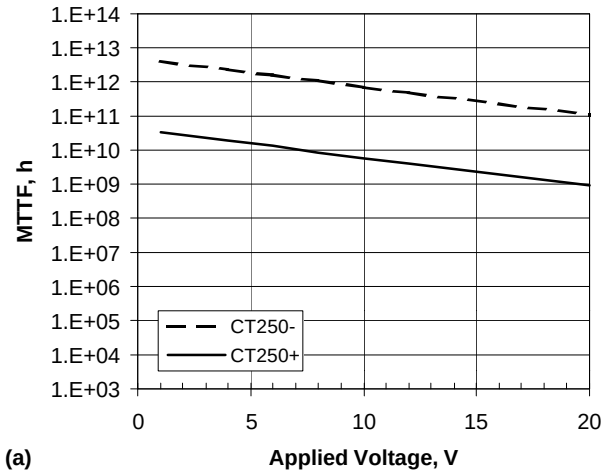
polarity:	+	+	+	–	–	–
type:	CT50	CT200	CT250	CT50	CT200	CT250
wafer A	35.3	35.6	59.5	38.2	44.2	44.6
wafer B	41.9	34.4	52.0	41.7	38.2	*
wafer C	38.4	38.9	26.8	41.7	47.8	43.5
wafer D	35.3	45.7	42.8	38.2	46.2	44.6
wafer E	38.2	37.5	38.2	38.2	36.5	*
average:	37.8	38.4	43.9	39.6	42.6	44.2

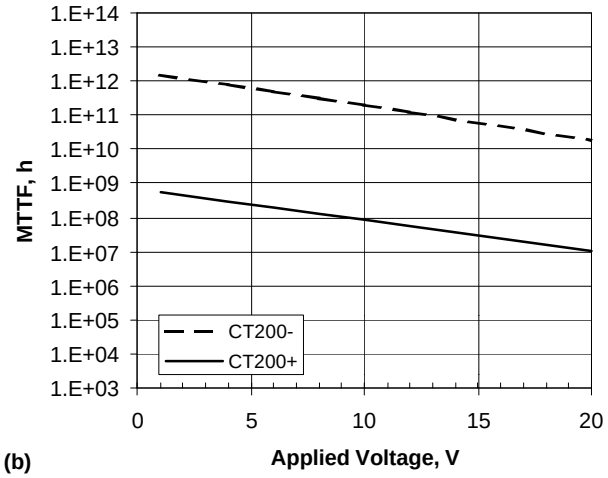
* values could not be estimated because test equipment limited to 200 V.

Figure 2 shows resulting lifetime predictions, using the lot average values of γ for each capacitor type and polarity. The predicted lifetime for CT200 and CT250 is more than 10^7 hours for operating voltages up to 20 V at both polarities. CT50 capacitors have lifetimes greater than 10^7 hours for operating biases of 4.0 V or less, and 10^6 hours for biases of 6.0 V or less. In practice, we limit the use of CT50 capacitors to applications with 6 V or less bias and to applications where 10^6 hours is acceptable. At lower voltages, the higher capacitance density of CT50 enables a significant reduction in circuit area. The other capacitor types can be used for larger voltages, up to 20 V. For all three types, the predicted lifetime for negative bias is considerably greater than that for positive bias. Where possible, designers using this process should arrange capacitor connections to apply negative bias to the top plate.

FIXED VOLTAGE MEASUREMENTS

A small sample of CT50 capacitors were tested manually at fixed voltages, selected for short lifetime. Figure 3 shows the resulting lifetime as a function of applied voltage using negative polarity. The data was fit with the linear field model, resulting in γ = 40.7 nm/V. Then, additional samples from a wafer with similar ramped voltage performance were put on extended time test at even lower voltages. These data points diverge from the prediction, in the direction of longer lifetimes. This is understandable for reasons described below.





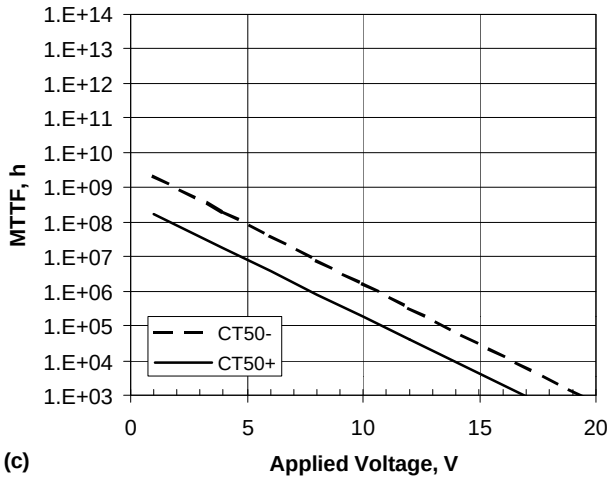


Fig. 2: Linear field model lifetime prediction, both polarities, for CT250 (a), CT200 (b), and CT50 (c).

Although the linear field model appears to be a reasonable basis for projecting operating lifetimes from ramped voltage data, it works best for high voltages. The linear field model specifies a functional form for the lifetime dependence on applied bias voltage V_A as

$$t(V_A) = A\exp(-BV_A) \qquad (4)$$

where A and B are constants. This form leads to finite lifetimes under zero stress conditions. A possible improvement is a model based on Frenkel-Poole conductivity [5], which has the functional form

$$t(V_A) = \frac{C}{V_A}\exp(-D\sqrt{V_A}) \qquad (5)$$

where C and D are constants. Such a functional form correctly predicts infinite lifetime at zero stress. Figure 3 includes a curve fit to the Frenkel-Poole model for the entire data set. Additional work is in progress to assess the different models at lower voltages.

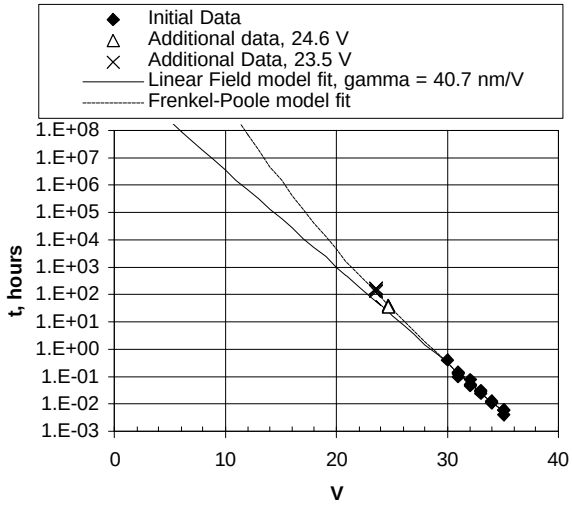


Fig. 3: Constant voltage stress lifetimes of CT50 capacitors, negative polarity, with linear field and Frenkel-Poole conduction model fits.

Additional work is also in progress to examine defect populations. Capacitor reliability is determined both by intrinsic reliability and by the distribution of defects such as included particles and metal evaporation splatters. Defect densities in mature GaAs MMIC processes are very low, and very large sample sizes are needed to detect and characterize these small populations.

CONCLUSIONS

A single GaAs MMIC fabrication flow can provide the designer with multiple options for capacitance densities. We have demonstrated reliable performance using 50 nm, 200 nm, and 250 nm silicon nitride. The linear field model for predicting capacitor lifetimes is used as a reasonable starting point. We believe that improved silicon nitride reliability models will predict even longer lifetimes at typical operating biases.

ACRONYMS

MIM: Metal-Insulator-Metal
pHEMT: pseudomorphic High Electron Mobility Transistor
PECVD: Plasma-Enhanced Chemical Vapor Deposition

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