Characterization of Electroplated Gold for Back-Side Processing of GaAs Wafers

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ABSTRACT

A statistical design of experiments (DOE) has been performed on an automated, fountain-type electroplating system to characterize the effects of current density, waveform, and agitation rate on the conformal coverage of deposited gold films onto the back-side surfaces of 100 mm diameter, thinned GaAs wafers. The goal of the DOE was to find optimal conditions that would give both conformal coverage and a high deposition rate.

Results show that increased agitation and decreased current density result in a more conformal plated film. This suggests that there is a reduced number of gold ions available for plating at the bottom of the via compared to the back-side surface due to mass transfer limitations.

INTRODUCTION

The recent increase in demand for III-V semiconductors devices over the past few years has made the automation of back-side processing steps desirable to improve yield and increase throughput. One of the important steps in back-side processing of GaAs wafers for power devices is the electrochemical deposition (ECD) of a conformal gold layer on the back-side surface and into through substrate via holes. The gold layer must be thick enough to provide mechanical strength to the thinned wafer and meet minimum thermal and electrical conductivity requirements. Conformal coverage of the plated gold inside the via holes is desired to meet the conductivity specifications without compromising plating throughput. It can also result in the deposition of a lower volume of precious metal than for non-conformal coverage.

For GaAs MMICs (monolithic microwave integrated circuits) power devices, through substrate via technology has been widely used in order to meet thermal conduction requirements and provide for low inductance ground connections.[1] Flip chip technology for GaAs MMICs[2-5] is an alternative to through substrate vias, but has been slow to gain wide acceptance with GaAs device products thus far. One reason for this may be the capital outlay required for new equipment needed for flip chip die bonding to modules and boards. However, it is expected that the adoption of flip chip technology by III-V semiconductor facilities will grow in the near future as equipment cost of ownership (CoO) decreases and yield improves. The future of through substrate via technology for compound semiconductors will ultimately be driven by cost, so yield, equipment throughput, and overall process cycle time will continue to be key factors.

Most articles written over the years covering through substrate via technology have focused on device performance and plasma etching.[1, 6-16] Recently, an article was published that discussed the use of long throw and collimated sputtering to achieve improved seed layer coverage within high aspect ratio vias.[17] Gold electrochemical deposition of compound semiconductor through substrate vias has not been covered as extensively as plasma etching.[1, 18, 19]

As through substrate via size has decreased and aspect ratio increased in order to allow for reduced die sizes, further demands have been placed on the gold ECD process step. Pulse plating has been shown to result in decreased grain size, lower stress, and higher throwing power compared to conventional DC plating.[20-22] As GaAs wafer production volumes have increased, the gold ECD step has been moved from low throughput, single-wafer bath set-ups to much higher throughput, more automated wafer plating tools. An optimized gold ECD process must meet thermal and electrical requirements, have a high plating rate, and achieve close to conformal coverage over the back-side surface and inside the vias. The electrodeposited gold layer also provides mechanical strength to the thinned wafer.

EXPERIMENTAL

A lot of pHEMT GaAs power device wafers that went through front-side wafer processing and were rejected at final front-side electrical test was used for the DOE. The 100 mm diameter wafers were mounted on 103.4 mm diameter, non-perforated sapphire carriers using Staystik 336T spin-on thermoplastic adhesive.[23] The temporary wafer / carrier bonding was performed in a batch Sharon Vacuum bonding tool employing spring loaded pressure

plates, a programmable heating element, and a mechanical pump.[18] The wafers were thinned to a 100 µm target thickness by first grinding on a single spindle, batch G&N 400 wafer grinder. Then the grinding damage was removed by polishing on a batch Speedfam wafer polisher.

A 10 µm thick, single coat of AZP4620 positive photoresist was spun on the wafer back-sides and hotplate baked using a MTI photo-track with custom made, over-sized wafer cassettes. A Karl Suss MA150 Back-side IR mask aligner was used to expose the via contact mask. After develop and inspection, the thinned wafer / carriers were loaded into a Plasma Therm SLR720 RIE system with a loadlock. After a short oxygen plasma descum, a two step BCl_3/Cl_2 etch recipe was used to etch high aspect ratio via holes to 100 µm square front-side, evaporated Ti/Pt/Au ground pads.[24] The photomask was stripped in 55°C ACT1-NA from Ashland Chemical followed by a DI water rinse and dry. Residual organics were removed by an oxygen RIE recipe in a second Plasma Therm SLR720 system. The GaAs back-side surface was roughened slightly and the oxide layer removed by wet chemical treatments. A 50 nm TiW / 200 nm Au seed layer was deposited in a batch, magnetron MRC sputtering system.

A Semitool fountain-type system was used for electrochemical deposition (ECD) with a commercially available gold sulfite-based plating solution. All wafers were plated to a target thickness of 3.0 µm.

Two rounds of experiments were performed with the first investigating the effect of plating current density on the conformality of the gold film. Current densities of 1.0, 2.5, and 4.0mA/cm^2 were investigated using a pulsed waveform with a 25% duty cycle at 833Hz. Conformality is defined as the ratio of the plated thickness at the bottom of the vias to the plated thickness on the back-side surface.

The second experiment focused on the effect of frequency, duty cycle, and agitation at a constant current density of 2.5mA/cm^2 on conformality. Agitation is defined as the combination of plating solution flow rate and wafer rotation rate.

RESULTS

Current density proved to have a large effect on the conformality of the plated film. Lower current densities resulted in a more conformal deposit. Table 1 below outlines the results obtained from the first round of experiments. Two wafers were processed at each of the three different current densities.

Table 1: Conformality results for varied current densities

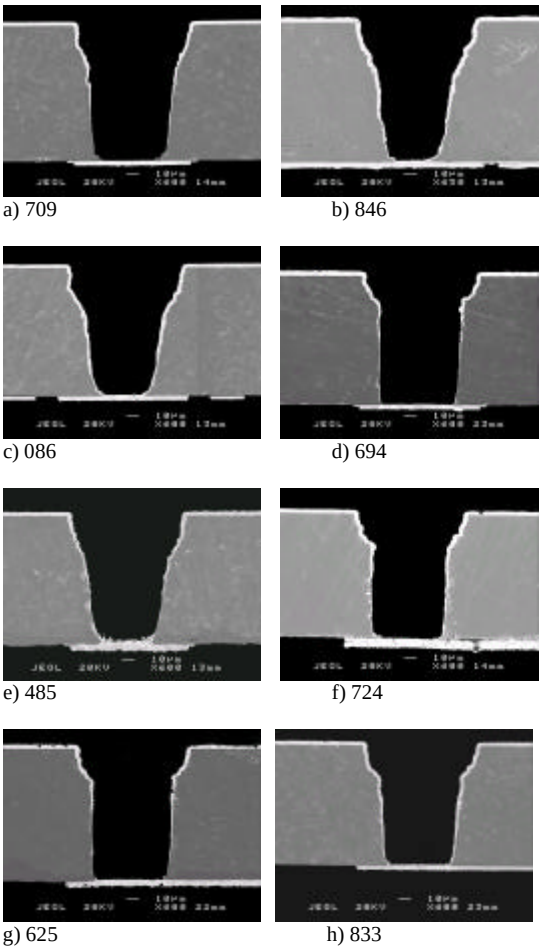
	1.0 mA/cm^2	2.5 mA/cm^2	4.0 mA/cm^2
Run 1	0.67	0.33	0.13
Run 2	0.50	0.23	0.08

Desirable results were obtained at 1.0mA/cm^2. However, a higher plating rate is preferred for a high throughput, production process. Therefore, a two level / three factor statistically designed experiment was performed to find parameters to improve conformal coverage at higher current densities. After processing the wafers, SEM cross-sections were performed and thickness measurements were made to determine the conformality of the plated film. The measurements were made on via hole cross sections taken from the center and the edge of the wafer. Table 2 outlines the statistically designed experiment along with the results obtained for wafer edge measurements.

Table 2: DOE plating conditions and results for the eight wafers mounted on carriers.

Wafer ID	Pattern	Agitation	Duty Cycle	Frequency	Conformality
625	---	-1	10	1000	0.09
485	--+	-1	10	100	0.15
694	-+-	-1	50	1000	0.09
709	-++	-1	50	100	0.09
86	+--	1	10	1000	0.55
833	+-+	1	10	100	0.33
724	++-	1	50	1000	0.31
846	+++	1	50	100	0.36

Figure 1: Cross section SEM photos of through substrate vias taken from the edge of each of the 8 wafers. See Table 2 for the plating conditions. The GaAs thickness is about 100 µm and the front-side pad (bottom of the photos) width is 100 µm.



a) 709 b) 846

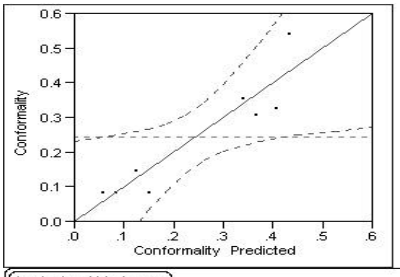
c) 086 d) 694

e) 485 f) 724

g) 625 h) 833

A standard least squares regression analysis was performed using JMP statistical software package to determine which parameters had an effect on the plating conformality. Figure 2 shows the results of the regression analysis performed for the wafer edge data.

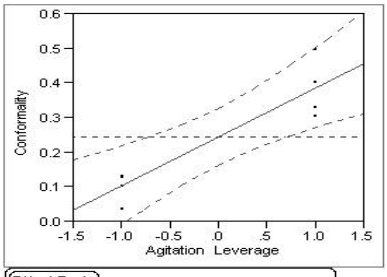
Figure 2: Regression analysis results (leverage plots)



Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	3	0.17151659	0.057172	8.2808
Error	4	0.02761662	0.006904	Prob>F
C Total	7	0.19913321		0.0343

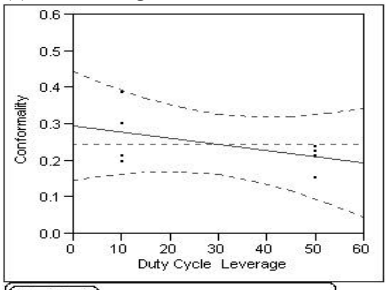
(a) Whole Model Test



Effect Test

Sum of Squares	F Ratio	DF	Prob>F
0.16117003	23.3439	1	0.0085

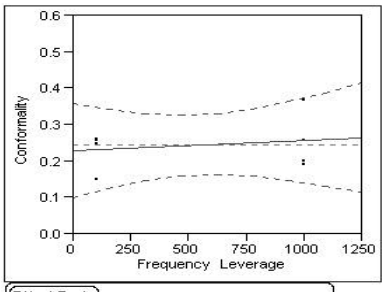
(b) Effect of agitation



Effect Test

Sum of Squares	F Ratio	DF	Prob>F
0.00903840	1.3091	1	0.3164

(c) Effect of duty cycle



Effect Test

Sum of Squares	F Ratio	DF	Prob>F
0.00130816	0.1895	1	0.6858

(d) Effect of frequency

Leverage plots and the Prob>F value give a good idea of whether or not a factor has an effect on the response variable. A Prob>F less than 0.05 is evidence in the Whole-Model Test that at least one of the factors being investigated has an effect on the response variable. Further evidence that at least one of the factors has an effect on the response variable is displayed in the leverage plot for the Whole-Model Test. If the 95% confidence intervals, represented by the dashed curves, intersect the mean of the response (0.24 represented by dashed line) there is evidence that there is at least one significant factor in the model.[25]

Figure 2(a) shows a leverage plot for the Whole Model Test. A Prob>F value of ~0.03 and the fact that the confidence interval intersects the mean of the response is evidence that at least one of the factors investigated has a significant effect on conformality.

To determine which of the factors investigated has an effect on the conformality the same analysis is performed on the leverage plots for the individual factors. The leverage plot for agitation vs. conformality has a Prob>F value of 0.0085 (<0.05) and a high F-Ratio of 23 (compared to the other two factors). The 95% confidence interval curves intersect the mean response indicating that the agitation rate has an effect on the conformality of the plated film. Leverage plots and Prob>F values for the duty cycle and frequency factors do not present evidence of an effect on conformality in the ranges investigated.

The conformality of the plated film improves with increased agitation and decreased current density. This suggests that there is a reduced number of gold ions available for plating at the bottom of the via compared to the back-side surface due to mass transfer limitations.

SUMMARY

Two rounds of experiments were performed to determine optimal process conditions for gold electroplating for back-side processing of GaAs wafers. The goal of the experiments was achieving a conformal gold plated film in the back-side via. The first experiment investigated the effect of plating current density on the conformality of the plated film. Results indicate that decreasing current density improves the conformality of the plated film.

A statistically designed experiment was performed to characterize the effects of frequency, duty cycle, and agitation rate on the conformality of the plated film. Results show that increasing the agitation rate improves the conformality of the plated film while the frequency and duty cycle did not show an effect over the ranges investigated.

The results obtained in these two experiments suggest that there is a reduced number of gold ions available for plating in the bottom of the via compared to the back-side surface due to mass transfer limitations.

Further experimentation should focus on understanding the effects of mass transfer and charge transfer on the non-conformality of the gold plated film.

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