Methods for Monitoring Passivation Ledges in a Manufacturing Environment

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Abstract

In this paper, we present three techniques used to evaluate and monitor the hetero-guard ring (passivation ledge) properties of AlGaAs/GaAs HBTs. The techniques are simple enough that they are suitable for routine monitoring in a manufacturing environment.

INTRODUCTION

A common accepted passivation practice, for AlGaAs HBTs, is to leave a hetero-guard ring or "ledge" of thin depleted emitter layer on the extrinsic GaAs base surface. This ledge reduces the recombination current (allowing better scaling of devices) and improves the reliability [1-3]. A schematic view of the ledge region is shown in Fig. 1. While there have been many studies of the passivation ledge, very little work has been done to develop practical methods for monitoring it in a production environment.

In this paper, we present three techniques to monitor the ledge passivation for our non self-aligned AlGaAs HBT process. The first technique we present, "effective area ratio", provides an intuitive identification of the passivation quality by measuring devices with different ledge lengths and extracting the effective electrical area. This method also exposes a common misinterpretation about ledge operation. The second technique is the ledge CV and it offers a direct measurement of the ledge thickness by using an MIS-like Metal/Ledge/Base capacitor structure. The third method, "on-ledge potentiometer" technique [4], provides a quick determination of the passivation quality using an on ledge Schottky diode. These techniques can be useful as monitors in a manufacturing environment.

TECHNIQUE I - EFFECTIVE AREA RATIO (EAR)

The first technique, effective area ratio, relies on the fact that I_c (the collector current) is proportional to the emitter area, A_E. As given by:

$$I_c = J_s A_E e^{qV_{be}/nkT}$$

Where J_s is the saturation current density and A_E is the emitter area.

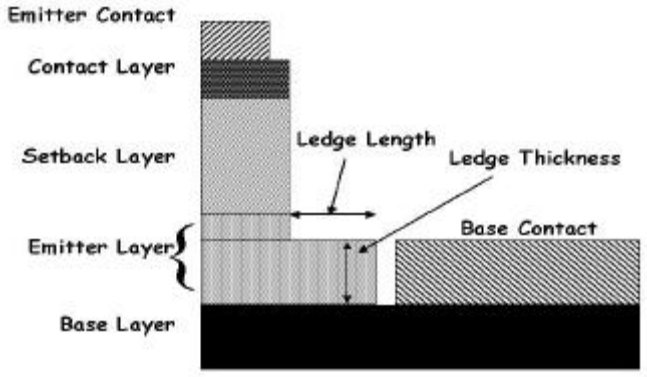


Figure 1. Schematic Of Ledge Region of an HBT

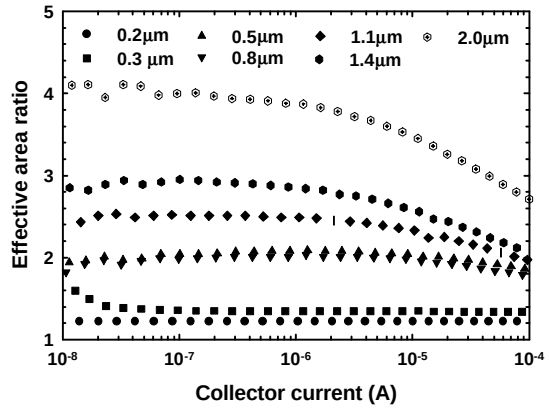
The first step is to measure an HBT with a low P/A ratio and divide by emitter area to find J_s (which only depends on material parameters to first order). We then multiply this J_s by the drawn-area of the small area device we are measuring (with different ledge lengths) to find the "ideal current":

$$I_{ideal} = I_{S,large} \frac{A_{small\ device}}{A_{large\ device}}$$

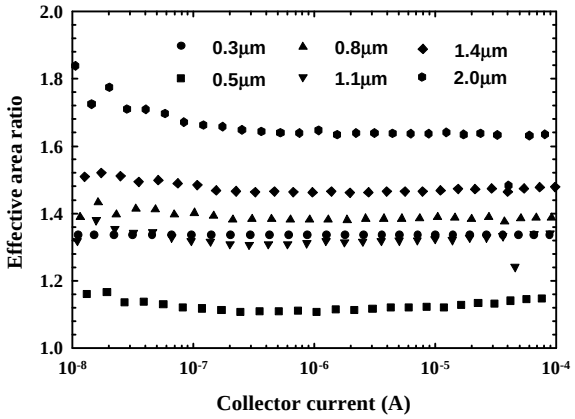
The effective area ratio (EAR):

$$EAR = \frac{I_{measured}}{I_{ideal}} = \frac{J_s A_{measured}}{J_s A_{ideal}} = \frac{A_{measured}}{A_{ideal}}$$

Is defined as the measured current divided by this ideal current, as shown in Figs. 2a and b. The first observation from this figure is that devices with larger ledges (that are not functioning properly) have very large effective areas at low current. This means that the devices with bigger ledges actually have higher collector and bases currents than they should. The base current displaying this behavior is counter to the idea that a larger ledge provides less base current (higher DC gain) at low bias. At high currents, the larger ledge does, indeed, provide a higher peak DC gain. A



(a)



(b)

Figure 2. Examples of Effective Area Ratio Measurements for 4 μm^2 devices

second observation from Fig. 2a is that the effective device area decreases dynamically as I_c increases. In Fig. 2b, we show the same measurement for a well-designed ledge. Note that there is little dependence of the effective area ratio on bias for this emitter structure and that the ratio is closer to one (meaning the current is behaving more ideally). This decrease in effective area is in direct contrast to the way most authors have described ledge behavior (the idea of the ledge becoming less pinched off)[5], but is simply understood using a distributed model for the base-emitter of the HBT [6], as shown in Fig. 3. At low bias, the poorly designed ledge allows injection of emitter current across the entire emitter, including the ledge. As more current flows from the emitter into the base, the junction resistance in the intrinsic region is decreased (making it easier for current to flow there). In the ledge region, there is an IR drop that causes a lower effective turn-on as we move away from the intrinsic emitter, so a lower percentage of the current actually flows in the ledge region, similar to current crowding. This has been verified by two-dimensional device simulations and through sub-circuit simulation using SPICE. For a properly designed ledge, the resistance across the ledge (from it being either fully depleted or almost fully depleted keeps most of

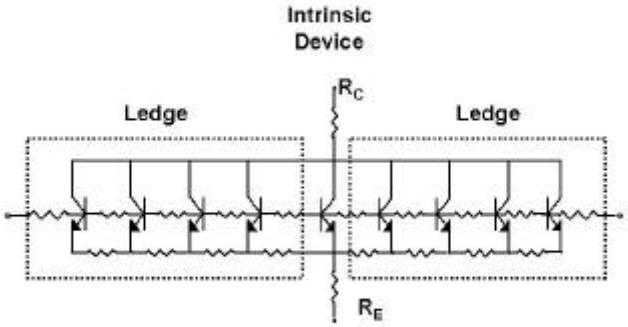


Figure 3. Equivalent circuit representation of HBT with ledge

the current flowing from directly under the intrinsic emitter, making the effective area approximately equal to the intrinsic emitter area. For in-line monitoring, it is generally sufficient to compare the EAR of a short ledge device to a long ledge device.

TECHNIQUE II - LEDGE CV

The second technique, is referred to as "ledge CV", and uses a simple MIS capacitor made from M1/ledge/base, as shown schematically in Fig. 4. Using the simple relationship:

$$C = \frac{\varepsilon_s A}{d},$$

provides a direct monitor of the fabricated ledge thickness. A sample CV curve (from a test wafer) from this structure is shown in Fig. 5. This structure is routinely monitored in our process line by simply measuring the zero bias capacitance, as shown in Fig. 5. The thickness from

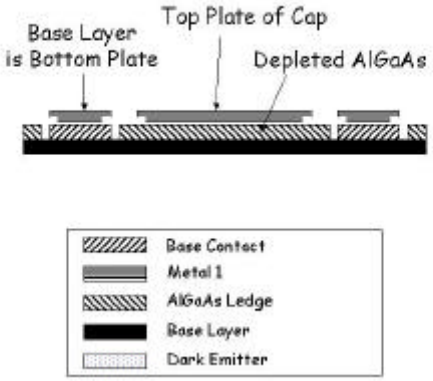


Figure 4. Schematic of Ledge CV structure

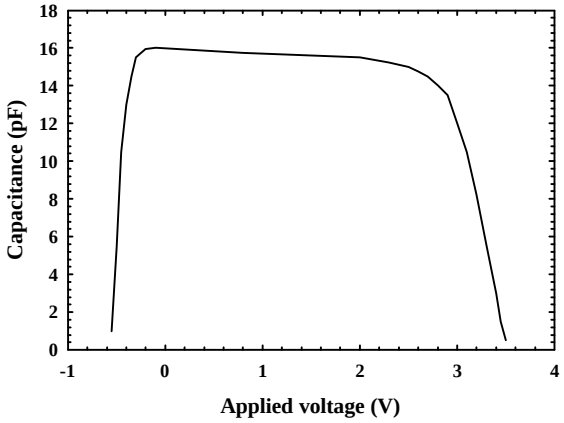


Figure 5. Data from Ledge CV measurement for 200/600 Structure

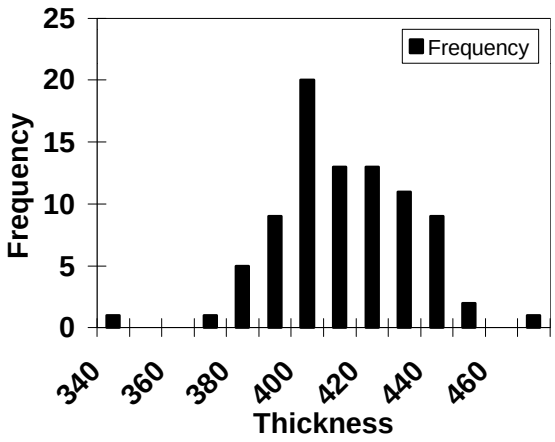


Figure 6. Ledge CV results from a single wafer lot, multiple sites per wafer. Thickness is in Angstroms

this measurement is in good agreement with SEM cross-sections. An additional measurement that can be performed using this structure is a diode I-V. If the ledge becomes too thin, this MIS diode has a very low turn-on since it essentially becomes a p-type Schottky with the barrier lowered by the n-type AlGaAs. This IV measurement is also helpful in setting the voltage swing used in the CV measurement, depending on the ledge thicknesses used.

TECHNIQUE III - ON-LEDGE SCHOTTKY DIODE

Finally, the third technique/structure for monitoring the passivation ledge is a Schottky potentiometer [4]. A top view of the layout for this structure is shown in Fig. 7. On the ledge of the HBT, we place a Schottky contact, formed by removing the passivation nitride and contacting with first interconnect metal. Since Au is used as the contact metal, the Fermi level of the surface is pinned close to the center of the band gap, as it would be if passivated with a dielectric.

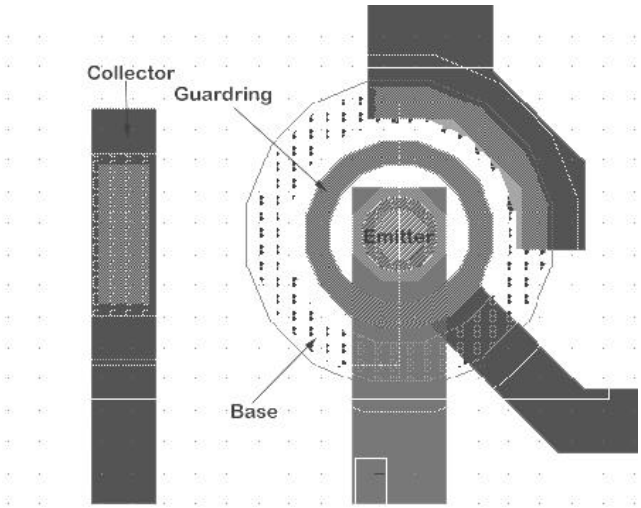


Figure 7 – Top View of Guard-ring Device

The simplest measurement for monitoring the passivation quality is to force zero current into the Schottky contact and then performing a normal Gummel plot measurement. The ledge voltage, L_{edge}, is then plotted against the base-emitter voltage. If the ledge conducts, the ledge voltage no longer follows the V_{be}, as shown in Fig. 8 for the "un-pinched" ledge. Empirically (and from 2D simulations), better pinched off ledges have this breakpoint occur at higher V_{be} (also shown in Fig. 8). Also shown in the figure are the collector currents for these structures. The same measurement using an ohmic contact (basically a second emitter in place of the Schottky guard ring) on the ledge does not allow for an accurate determination of the passivation ledge functionality. The slight ramp in V_{Ledge} for the ohmic contact at higher V_{be} indicates that the current flow is beginning to flow predominantly under the intrinsic device and is consistent with the effective area ratio discussion above. Furthermore, the collector current for the ohmic contact reveals that it has almost identical behavior to the devices evaluated for the EAR measurements.

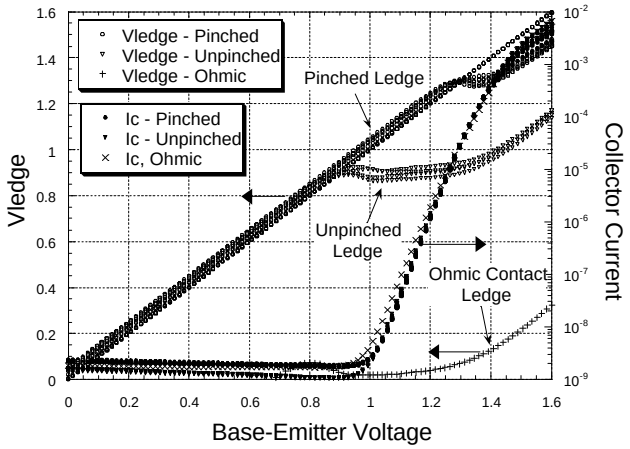


Figure 8 – Results of On-ledge potentiometer measurements.

CONCLUSIONS

In this paper we presented three measurement techniques/structures for monitoring the passivation ledge. These methods are all suitable for a manufacturing environment. These structures allow for an assessment of passivation ledge characteristics or optimization of the ledge design and can serve as early screens for potential reliability or process related device degradation.

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ACRONYMS

MIS- Metal/Insulator/Semiconductor
HBT- Heterojunction Bipolar Transistor
P/A-Perimeter to Area Ratio
CV – capacitance versus voltage
I-V – current versus voltage
V_{be}-base emitter voltage