Film Stress versus Plating Rate for Pulse-Plated Gold

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Abstract

Many compound semiconductor processes use plating to fabricate interconnect lines, bond pads, and transmission lines. As integrated circuit density rises, more concern is being paid to stress of the interconnect metalization. Residual stress in plated metal can affect the high frequency characteristics of devices such as inductors or transmission lines built up by the plating.

The internal stress of gold produced by electrodeposition was studied as a function of deposition rate for fixed film thicknesses. The gold plating solution was a sulfite formulation and the pulsed-plating mode was used to create deposits of 2 µm nominal thickness. The film stress was measured by laser scanning technology. The plating rate, at which the stress transitions from compressive to tensile, was determined experimentally.

INTRODUCTION

Many advances have been made in lithographic equipment and materials enabling an overall reduction in feature size. This reduction has lead to both increased circuit density and improved performance. However, the requirement of thick top interconnect metal (2-5 µm) remains the same due to the need for probe contacting to electrically test the circuit and for bonding of off-chip components. At the same time the fabrication of multilevel interconnect lines requires precise control of thinner metal films (1-2 µm). Electrodeposition has been demonstrated to be cost effective and capable of SPC for these applications.

The High Speed Circuits Laboratory (HSCL) at HRL Labs is responsible for gold plating of all advanced circuits fabricated on compound semiconductor materials. The plating operation is used to build up the thickness of the circuit traces, to construct air-bridges connecting traces, and to fill vias between circuit levels. [1] The process must provide thickness uniformity, high definition of critical dimensions, and reliable metal adhesion of circuits and integrated passive components.

BACKGROUND

The plating rate is determined by the affect of current passed through the metal-carrying electrolyte. The plating rate is the total thickness divided by the total time of deposition. In addition, the rate for a partial thickness is assumed to be the same as that for a full thickness deposition. This allows the time calculation to be made to achieve the final thickness. The predictability of thickness, by calculation of the required time from the rate determination, is key to repeatability. Plating at the same rate allows for quality control of the deposit. Any abnormalities may then be attributed to changes in bath chemistry or preparation of the plating surface.

Faraday's second law is used to calculate the metal deposited relative to the amount of current (amps) passed through the cell, times the amount of time (seconds) the current is applied.

$$\alpha_F * I * t = m = \rho * T * A \qquad [1]$$

Where,

α_F = (mole weight/ valence)/96,500 g/C.
ρ = Density of the plated material [g/cm^3]
A = Total plating area [cm^2]
t = Total plating time [sec]
T = Final plating thickness [cm]
I = Plating current [A]
m = Total mass of metal deposited [g]

Assuming we have a 100% efficient bath, we may write Faraday's law in the following form:

$$I / A = (\rho / \alpha_F) * (T / t) \qquad [2]$$

Equation 2 shows that, the current density (I / A) is directly proportional to the rate of deposition (T / t).

EXPERIMENTAL PROCEDURE

We used a commercially available sulfite gold plating solution and followed the process that was recommended by the vendor. A platinized mesh anode was used and the anode area was much larger than the cathode area. The cathode area was determined by photoresist patterning and the anode mesh was unmasked. The anode area spans the entire 3-inch circuit wafer. Plating robbers, brighteners, and alloying additives were not used.

Controlled parameters are plating current, time, pulse duty cycle, and temperature. Reliability metrics are plating rate and film stress. In microelectronic wafer fabrication it is desirable to specify a range for plating rate which yields acceptable film stress. The goal is to produce films of near neutral to slightly compressive stress. Tensile films are not acceptable due to increased risk of film delamination.

Equation 2 above requires knowledge of the total plating area. In this experiment, the wafer area outside of the plating pattern was masked completely to the substrate edge. Variability in the masking of the substrate can affect process control. For practical reasons, the plating pattern is printed past the edge of the substrate. If done with photolithography wafer stepper, this may result in acceptable repeatability. However, it may be difficult to calculate or accurately approximate the plating area. Most photolithography tool vendors will be able to report the printed area in the plating pattern of one reticle, which is then repeated on the wafer. This does make it possible, yet perhaps laborious, to accurately determine the total plating area.

If the plating area is unknown, then determining the plating current requires a recursive method. For example: test plating may be made with an arbitrary current and time; the resulting thickness is measured, and the test rate calculated. This may be repeated until the resulting test rate compares favorably with the specified plating rate (also, a specific plating rate may be calculated from the recommended current density using equation 2).

When the required throughput of the process increases to make customizing plating parameters for each substrate undesirable, then the plating parameters for each printed pattern may be characterized. These parameters would then be applied to all substrates in the production lot. This could allow for statistical averaging of the plating parameters to achieve the desired SPC. Deposition would be in a single run, and not in multiple runs, as mentioned above. This could not only improve the uniformity of the metal properties. And, as required by increased throughput, reduce handling. It should be mentioned, also that, when the risk of damage due to excess handling is a concern, it may be beneficial to deposit in a single run, using the same parameters on each substrate, and without interrupting the process to check thickness. Furthermore, abnormalities in the plating results could be more easily attributable to the appropriate causes.

STRESS MEASUREMENT

Measurements were taken on the FSM 128, from Frontier Semiconductor Measurement, Inc. The substrates used were ultra-flat 3 inch diameter Si(100), with both sides polished. The plating membrane was evaporated Ti(500 Å)/Au(1000 Å). The wafers were backside masked and edge clipped for electrical contact. Plating thickness was measured with an Alpha Step surface profilometer. Wafer thickness was measured with a height gauge. The initial FSM scan was made after plating membrane deposition, the final scan was made after plating. Three wafers were plated and measured at each rate.

It has been reported that the residual stress of the plated gold can be controlled in non-cyanide baths [3,4]. The operating parameters of commercial gold sulfite baths have been reported with special attention given to the effect of plating temperature and current density on residual stress in the deposited metal. Figure 1 shows the stress change from compressive to tensile as the current is raised [5]. This data is for DC-plating. It appears that the current density range for compressive stress is approximately 2 to 5.5 mA/cm^2. This corresponds to a D.C. plating rate range of approximately 450 to 1250 Å/min.

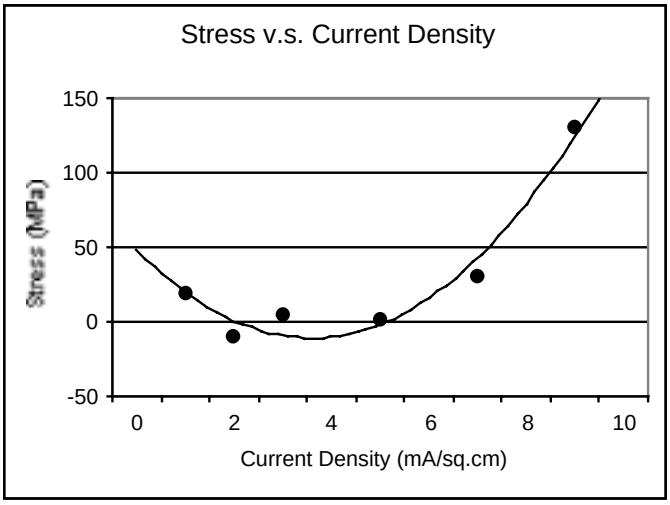

Figure 1.
Measured stress (dyne/cm^2) versus plating rate (Å/min). Negative readings are compressive, while positive readings are tensile. Film stress transitions from compressive to tensile above 1350Å/min, or 6 mA/cm^2. Tensile stress was not observed at rates below this value.

Reports of deposits plated at 1-2 mA/cm^2 DC without brightening agents at 50-60°C have internal stress measured to be in the range of 10^8 – 10^9 dynes/cm^2, compressive. [2] This is equivalent to a stress range of 10-100 MPa.

Plating rates used in our experiment were 200, 500, 800, 950, 1200, 1400, and 1850 Å/min. The resultant average thickness was 2.007 µm (+ 23%, -11%).

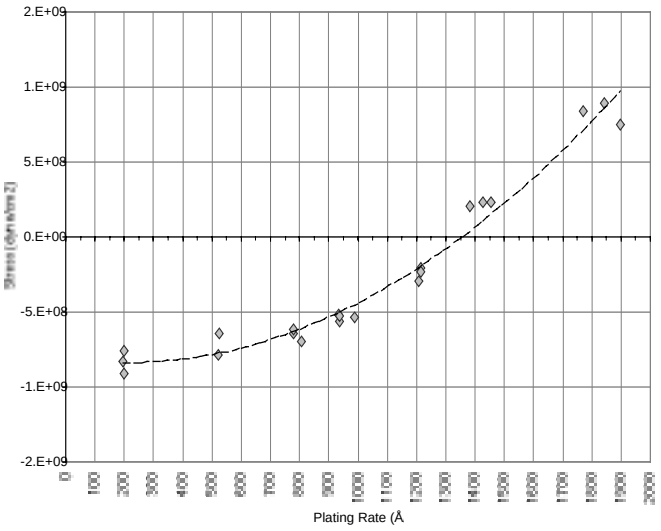

Figure 2.
Measured stress in dyne/cm^2 (Y-axis) versus plating rate in Å/min (X-axis). Negative values of stress are compressive, while positive values are tensile. Film stress transitions from compressive to tensile above 1350Å/min, or 6 mA/cm^2. Tensile stress was not observed at rates below this value.

CONCLUSIONS

It has been shown that pulse plating used with sulfite gold chemistry can result in a broad operating range. Stress measurements indicate near-neutral compressive stresses between 200 and 1200 Å/min. The associated compressive stress range is -9.09 x10^8 to –2.03x10^8 dyne/cm^2 or -90.9 to –20.3 MPa.

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ACRONYMS

HBT: heterojunction bipolar transistor
SPC: statistical process control
DC: direct current