Design of Experiments to Achieve High Yield Manufacturing at 6-inch Foundry

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Abstract

Four examples of process capability improvement at WIN Semiconductors were demonstrated by using various statistical techniques. 0.35um pHEMT gate lithography process was improved by using Bayesian methodology to achieve more than 1.0μm DOF (depth of focus) and good CD control. A DOE with Taguchi analysis method was utilized to find the optimal implant isolation condition in HBT for achieving low and consistent isolation leakage current. By using the optimum metal thickness and alloy conditions, a low and stable HBT base Ohmic contact resistance was accomplished. DOE with ANOVA analysis have also been carried out for the scribe and break process to find the optimal scribing force and angle. All the optimized process has been implemented in WIN's production line to produce high performance and high yield HBT and pHEMT MMICs.

INTRODUCTION

WIN Semiconductors provides dedicated HBT and pHEMT foundry service with advanced 6-inch MMIC process technologies. High quality, high yield, and cost effective manufacturing is the key for a successful foundry. Statistical approaches including the Design of Experiments (DOE) have been a staple of semiconductor manufacturing, therefore, engineers at WIN has applied DOE techniques in all process areas to screen the process variables, find the process windows, optimize key parameters, and then innovate repeatable, stable and high yield process technologies. In this paper, we demonstrate four examples of using statistical techniques to improve the process capabilities. They cover all the important process areas including photo, isolation, thin-film, and backside modules.

DOE DESIGN AND ANALYSIS

Several statistical techniques including Taguchi method, Analysis of Variance (ANOVA), and Bayesian variable selection methodology were utilized for this study. The Taguchi method defines two types of factors: control and noise factors. Taguchi recommends analyzing the mean response for each run in the inner array and analyzing variation using an appropriately chosen signal-to-noise ratio (SN), which is derived from quadratic loss function. The following equation is the SN formula to achieve "smaller the better" results,

$$SN = -10\log(\frac{1}{n}\sum_i Y_i^2),$$

where n is the sampling size and Y_i is the response at each sampling point. ANOVA table was used to find the significant factors from process variation. In many non-regular designs, the aliasing of effects has a complex pattern. It is difficult to disentangle the large number of aliased effects and to interpret their significance. Bayesian variable selection methodology [1-3] used in this study analyzes data with complex aliasing pattern and performs an efficient search for reasonable models. The interactions can therefore be estimated with reasonable precision.

DOE ONE : 0.35um GATE LITHOGRAPHY

Photolithography with lift-off structure has been the key process used in GaAs MMIC industry. However, the reproducibly and CD control for a small feature (< 0.5 um) is still a challenge. This becomes more complicated at the pHEMT optical gate process, which requires an excellent CD control to achieve uniform device performance. Furthermore, the big profile step variation at the gate recess area requires good depth of focus (DOF) photo process due to non-uniform photo resist thickness. Therefore, an improvement in 0.35um gate lithography process was initiated using DOE in an attempt to increase DOF and exposure latitude process window.

1.1) Experimental Procedure and Results

Three series of experiments were carried out to investigate the effects of 8 factors, each at 3 levels (Table I). The objective of the first two series in this study is to perform screening designs for model selection. On these two stages, experiments were conducted using blank wafers. The objective of the last stage is to confirm the prediction of these models and further optimize the processes on wafers with multiple layers of structures. An 18-run mixed-level-orthogonal array, L18 ($2^1 \times 3^6$), as shown in Table I, is selected because this design can study the

quadratic effects of each factor, and greatly reduce the number of runs required to perform an experiment. Method of sliding levels is also used to avoid bad regions in experimental space, such as a low temperature – short time or high temperature – long time combination.

Table I. Factors and levels of the first DOE.

		1	2	3
B	Soaking time	Level 1	Level 2	Level 3
C	Soft bake temperature (°C)	70	80	90
D	Soft bake time (sec)	Table II	Table II	Table II
E	Post exposure bake temperature (°C)	100	120	140
F	Post exposure bake (PEB) time (sec)	Table II	Table II	Table II
G	Coating speed (rpm)	4000	4300	4600

Table II. Sliding level of factor D and F.

90	40	60	80		
C 80		60	80	100	
70			80	100	120

D

140	40	60	80		
E 120		60	80	100	
100			80	100	120

F

All wafers were fabricated according to the design matrix and the gate CD opening was then measured. Based on Bayesian variable selection methodology, we found that the higher PEB (post exposure bake) temperature provides smaller CD to meet 0.35um target. Also the level-3 soaking and 90-sec soft bake time can provide good DOF based on the experiment result. Hence, we fixed two variables of soaking and soft bake time, and orient the PEB tendency to higher temperature on the second series to ensure the CD in the 0.35um ranges and further optimize the CD and DOF. We then used L9 experimental matrix with 4 control variables, including coating speed, soft bake temperature, PEB time and temperature. After conducted the matrix and measurement, the Bayesian analysis and regression calculation resulted in a model to describe the DOE dependency. The following equation describes the DOF from this model (Fig.1): DOF=1.022+(0.6928*Fl*Gq). This model suggests that there is a significant interaction between Fl (linear effect of factor F, PEB time) and Gq (quadratic effect of factor G, coating speed). Coating speed can be recognized as a noise factor, since photo resist thickness varies on the structured wafers. To minimize DOF dispersion, one can exploit the interaction between control factor (PEB time) and noise factor (coating speed). Since PEB time is much easier to change, it's more economical to reduce dispersion than directly reducing the photo resist (noise) variation. Hence, one can then choose PEB time at level 2 to have the flattest DOF response, as shown in Fig.1. Robustness can therefore be achieved.

To verify the above results, the optimal process conditions were applied to the structured wafers and the gate

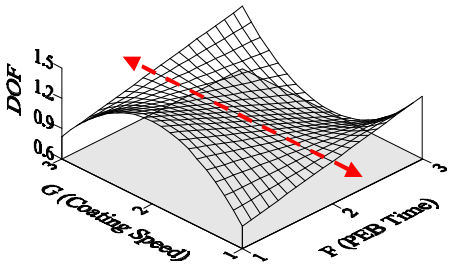

Figure 1 Response surface for DOF

CD opening was measured with the exposure focus varied from –0.2 to 0.8 with the best exposure energy. Table III shows a stable, highly reproducible CD control and small variation with large focus latitude. Therefore, with the statistical techniques (DOE), we were able to achieve good DOF and CD control for 0.35 um gate lift-off photo process.

Table III. CD variation with focus variance after optimization

Focus	-0.2	0	0.2	0.4	0.6	0.8
CD Mean	0.359	0.367	0.367	0.356	0.366	0.375
Std Dev.	0.009	0.008	0.004	0.004	0.006	0.005

DOE TWO : HBT IMPLANT ISOLATION

Implantation isolation is used in our 1um and 2um HBT technologies. Five implant dose and energy are used to isolate deep active region. The original dose and energy conditions were chosen by an implant simulation tool, however, we found the isolation leakage was about 40 nA with large wafer to wafer variations (Fig. 3). Therefore, a DOE with Taguchi method was utilized to find the optimal implant condition for achieving lower and consistent isolation leakage current.

2.1) Experimental Procedure

Four factors were chosen, including the energy and implant dose for step 1 (lowest energy) and step 5 (highest energy), energy for step 2, and energy for step 4. The reason to focus on the implant step one and five is because they are to isolate surface and buffer layers, which might be the root cause for the high leakage current. The L9 matrix was generated based on these 4 factors with 3 levels to process wafers and measure the leakage current.

2.2) Analysis and Discussion

Taguchi data analysis method was utilized to find the higher S/N ratio for the lower isolation leakage current to determine the optimal condition. Based on these criteria, condition A3 (condition A at level 3), B1, C2 and D1 were chosen (Fig. 2). To check the reproducibility, another lot was processed with the original and optimal implant conditions and the leakage current was measured. The

variance analysis showed that the samples with optimal condition had a much lower leakage current (average 44.3 nA) compared to the original condition (average 22.7 nA). After implementing this new implant process, we were able to achieve the isolation leakage below 25 nA with excellent uniformity for more than 50 wafers in our Fab. (Fig. 3).

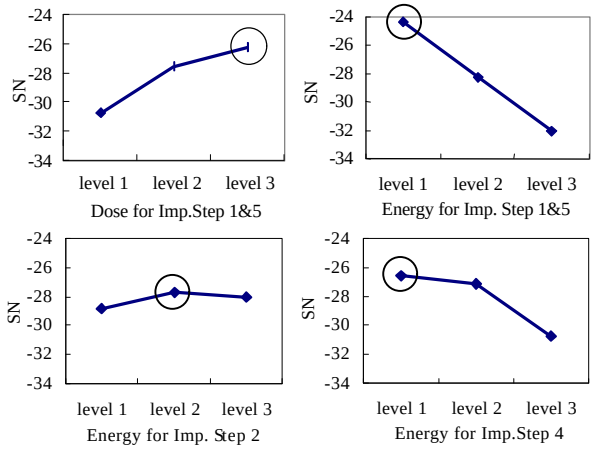

Figure 2 Optimal conditions were chosen based on S/N values

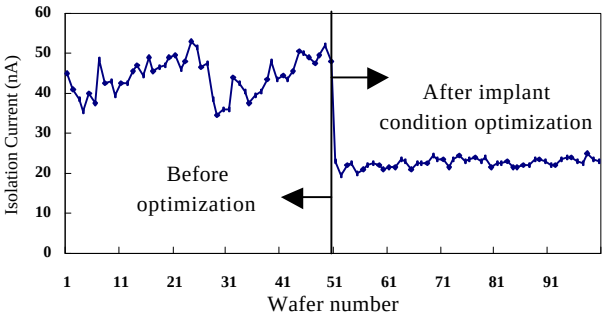

Figure 3 Great improvement in leakage and uniformity after DOE

DOE THREE : OHMIC CONTACT

A low and stable Ohmic contact resistance is critical to produce high performance and high yield MMICs. Our HBT base-metal contact process is to deposit Ti-Pt-Au multiple metal layers on p-type GaAs layer, then perform RTP alloy to achieve Ohmic contact. Before this study, we constantly encountered inconsistent contact resistance values, and sometimes open-circuit. Therefore, the optimization of the Ohmic process is necessary to achieve repeatable Ohmic contact and higher yield.

3.1) Experimental Procedure

Ohmic metal with various metal thickness was deposited and lifted of on the base region of the wafer after the Emitter mesa etch. RTP with various alloy conditions was performed after the metal formation. TLM patterns were used to measure the contact resistance (Rc) and sheet resistance (Rs) with HP4145. In this study, 4 factors were chosen for the design of experiment. They are (1) bottom metal thickness, (2) alloy temperature, (3) alloy time, and (4) temperature ramp up rate. DOE with Taguchi method was implemented with L9 matrix for four-factor with three-level design.

3.2) Analysis and Discussion

Taguchi data analysis method was utilized to find the higher S/N ratio for the lower Rs and Rc to determine the optimal condition (Fig. 4). The experimental results and analysis showed that the bottom metal thickness is the most critical factor to achieve lower contact and sheet resistance. The alloy temperature and time plays a second role on Rc and Rs. Contact resistance is not sensitive to the temperature ramping rate. Using the optimum thickness and alloy conditions, we were able to achieve consistent results in our production. Figure 5 shows our PCM SPC trend chart for HBT base Rc with an average of 0.13 (Ω-cm^2) and standard deviation of 0.02 with more than 80 wafer data.

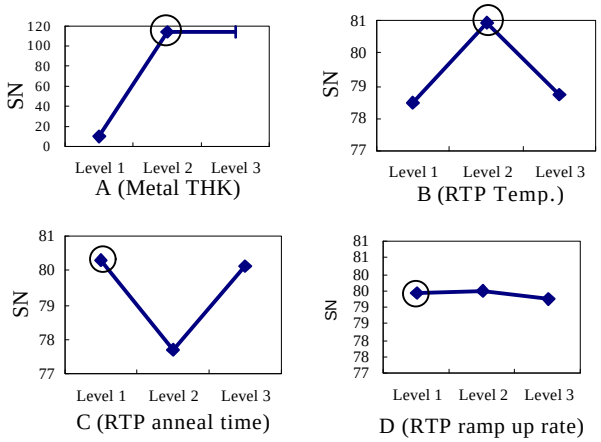

Figure 4 Optimal conditions were chosen based on S/N values

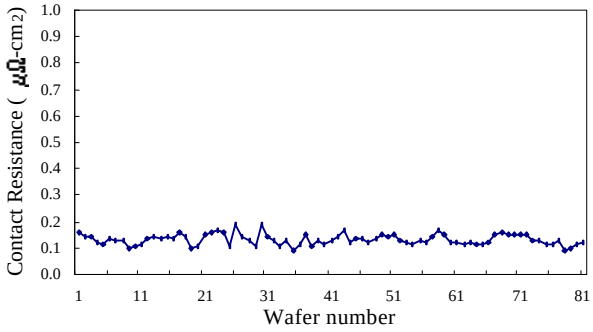

Figure 5 Base metal contact resistance SPC chart after optimization

DOE FOUR : SCRIBE AND BREAK

The yield in the scribe and break separation of GaAs wafers is very critical since the wafers are close to the end of

production. For scribing quality, serious chipping will generate the debris to containment the chip surface and moreover damage the device area. Two or more chips connected due to poor separation will reduce the yield directly. However, scribe and break is a complex process that involves the optimization of numerous parameters such as scribe force, diamond tool angle and speed, breaking force, breaking height and dwell time, and other machine dependent parameters. Furthermore, the scribe tool quality and life are also strongly affecting the dicing quality [4]. With so many variables, a design of experiments is apparently in place for process optimization. In this topic, DOE with Taguchi method have been carried out for the scribe and break process to find the optimal scribe force and scribe angle along the X and Y-axis.

4.1) Experimental Procedure

Three wafers were implemented with 18 various scribe and break conditions from angles and forces of X and Y-axes by DOE method, which is a combination of 4 factors (X-force, X-angle, Y-force, and Y-angle) and 3 levels. The whole experiment was carried out in one diamond tool (The tool life was keep in 75.2m~152.7m). We check the separation rate and the scribing quality for every condition on the wafers after the expanding process. The scribing quality was quantified by using visual inspection with a score system shown in figure 6.

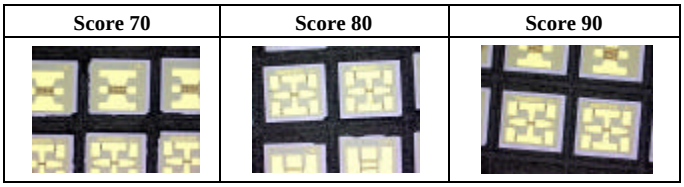

Figure 6 Visual inspection with a score system for scribe & break

4.2) Analysis and Discussion

The results of separation rate and scribing quality were analyzed by ANOVA method to find the significant factors. It was found that the Y-angle had the most significant impact (under 0.05 significant level) on the scribing quality. The interactions existed between Y-force and Y-angle to impact the scribing quality. The best condition to achieve highest scribing quality was Y-force and Y-angle both at level 2. As of the separation, X-angle had the most influence. No interaction was found between the four factors to impact the separation. By combining the above results and analysis, we concluded that the optimal condition to achieve high scribing quality and separation rate was X-force at level 1, X-angle at level 1, and both Y-force and Y-angle at level 2.

The optimal condition was implemented to check the repeatability on the scribe and break process. Figure 7 shows the results form five different runs, all in the range of 60-200 meter tool life. Most of the scribing was good with the score over 80 and the separation rates over 95%. Even though the DOE results were encouraging on the improvement of dicing quality, after implementing the optimal conditions, we still found intermittent cases with a lower scribing quality. We believe that the reasons for the inconsistency were probably due to other factors that are not included in this DOE, even though the force and angle are the common parameters tuned in the scribing machine. Therefore, with varying tool quality and life, care must be taken in order to obtain consistent results.

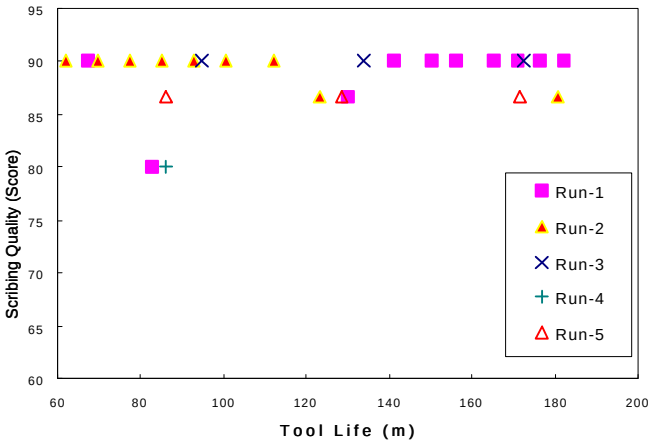

Figure 7 Good dicing quality (score over 80) for 5 runs after DOE

CONCLUSIONS

We have demonstrated four examples of using statistical techniques to improve the process. They include a 0.35 pHEMT gate lithography optimization, DOE for implant isolation to reduce leakage current, Ohmic contact process for better contact and sheet resistance, and the scribe and break process improvement by DOE. All the optimized process has been implemented in WIN's production line to produce high performance and high yield HBT and pHEMT MMICs.

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