High Yield InGaP HBT Manufacturing Technology on 150-mm GaAs Wafers

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Abstract

This paper reports on the high performance and high yield InGaP HBT manufacturing technology on 150-mm GaAs substrates developed at WIN Semiconductors. The high yield is due to the uniform and repeatable 6" epitaxial wafers, mature fabrication technology with wide process window, and state-of-the-art 6" process equipment. The device performance and reliability are also presented.

INTRODUCTION

GaAs HBT is the workhorse for today's cellular handset power transistors and one of the mainstream technologies for commercial wireless and lightwave communication circuits. Besides performance advantages, fabrication on 150-mm GaAs substrates makes GaAs HBT's much more cost competitive with other potential solutions. The transition from 4" to 6" GaAs substrates promises approximately a 40% processing cost reduction on a unit area basis [1-2]. Compared to AlGaAs HBT's, the InGaP-emitter HBT's have been shown to provide better reliability, better thermal stability, and is more scalable, which are essential characteristics for 3G handset PA's. This paper reports on the high performance and high yield 150-mm InGaP HBT manufacturing technology developed at WIN Semiconductors.

PROCESS TECHNOLOGY

In the 150-mm GaAs production line, there are two HBT processes - 2μm and 1μm HBT's -mainly targeting for wireless power amplifiers (cellular handset and WLAN) and OC-192 transceiver IC applications, respectively. The epitaxial layer structures feature MOCVD grown C-doped base, InGaAs emitter contact layer, mesa etch stop, and ledge layer. Two metal layers are provided for interconnection. The inter-layer dielectrics are SiN and polyimide for the 2μm process and 1μm process, respectively. 50Ω/ sputtered TaN is used for thin film resistors (TFR's). Ion implantation is employed for device isolation. MIM capacitors are realized with PECVD Si_3N_4 with unit capacitance of 300 pF/mm^2. Stack capacitors with unit capacitance of 450 pF/mm^2 are also provided to reduce the die size of MMIC for the 2μm process. While for the 1μm process, a unit capacitance of 600 pF/mm^2 is provided for MIM capacitor. The backside process features 100μm thick substrate, 50μm in diameter standard through via holes, gold plating and street etch. Totally there are 13 and 14 mask levels for the complete process of 2μm HBT and 1μm HBT, respectively. The Schottky diodes are also available for both processes. Fig. 1 shows a cross-section view of a finished 2μm unit transistor (2 emitter fingers, 3 base fingers). Fig. 2 shows the SEM photo (with polyimide removed) of a 1μm HBT with 2μm long emitter finger.

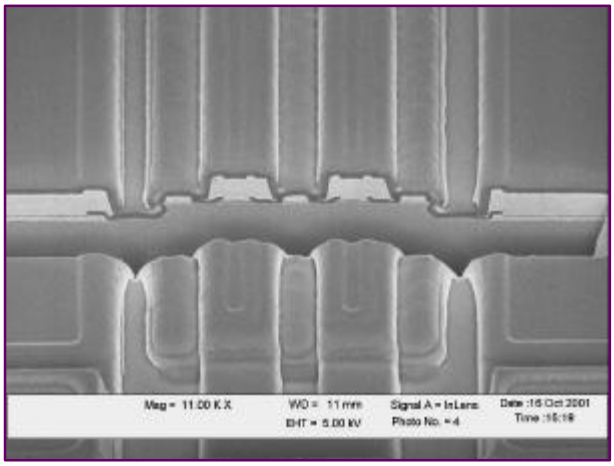

Fig. 1. Cross-sectional view of a finished 2μm HBT.

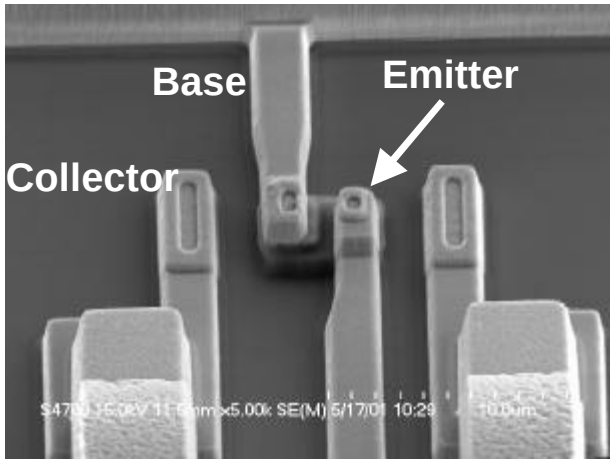

Fig. 2. SEM photo of a 1μm HBT with 2μm long emitter finger (with polyimide removed).

In-line process control is realized by constantly monitoring the critical layers in the lithography, etch, thin film, and backside process areas. In the lithography area, the photoresist thickness, critical dimensions, and photoresist liftoff profile are regularly monitored. The etch rates and etch profile for mesa, SiN and polyimide are carefully watched in the daily basis. SiN thickness and reflective index, TaN sheet resistance, metal (both ohmic and interconnect) thickness are also routinely monitored in the thin film area. In the backside process module, the controls of final wafer grinding thickness, through via hole etch rate, gold plating thickness and gold etch rate for streets are very essential and deserve special watch.

Process Control Module (PCM) is used to monitor the epitaxial material consistency, active and passive device electrical performances. Epitaxial material related parameters include the sheet resistances for emitter, base and sub-collector. For active device, the dc current gain (β), breakdown voltages, junction turn-on voltages, contact resistances, junction capacitances, and cutoff frequencies (f_T and f_{max}) are monitored to ensure the consistent HBT performance is obtained. For passive elements, the sheet resistance of thin film resistor, unit capacitance for MIM capacitor and isolation leakage current are also included in the PCM.

Fig. 3(a)-3(c) show the SPC charts on three most critical parameters as an example: dc current gain (β), E-B junction breakdown voltage, and current gain cutoff frequency f_T. Each wafer was tested at 25 locations across the 150-mm wafer. The average PCM yield >96% is routinely obtained. Taking data from 70 production lots (300 wafers) for the 2μm HBT process, the standard deviations for dc current gain, E-B junction breakdown voltage, and f_T are 5.1%, 3.8%, and 2.0%, respectively, indicating excellent uniformity and repeatability are achieved. A fab yield of 84% has been achieved in the 6" processing line by considering the wafer breakage yield, PCM yield, and visual inspection yield. The high yield is ascribed to the uniform and repeatable 6" epitaxial wafers, mature fabrication technologies with wide process window (by implementing Design of Experiments [3]), and the state-of-the-art 6" process equipment.

Fig. 4 shows the HBT power amplifier die yield mapping. For each die, 30 dc test points are measured. Within the 5mm wafer exclusion zone, 469 dies out of 46,853 dies fail (marked with dots), indicating a die yield as high as 99%. The laser marks (notch and its diagonal) are the most concentrated area with failed dies.

DEVICE PERFORMANCE

Table 1 summarizes the device performance for both 2μm and 1μm HBT processes. The 2μm HBT has a peak current gain of 80 and BV_{CEO}>12V (typically 15V). The peak f_T is about 35GHz at V_{CE}=3.6V and collector current density of 25-30KA/cm^2. The 1μm HBT has a peak current gain of 130 and BV_{CEO}>9V which is sufficient for lithium niobate modulator/laser driver applications in fiber optic communications. The peak f_T is about 65GHz at V_{CE}=1.5V and collector current density of 80KA/cm^2.

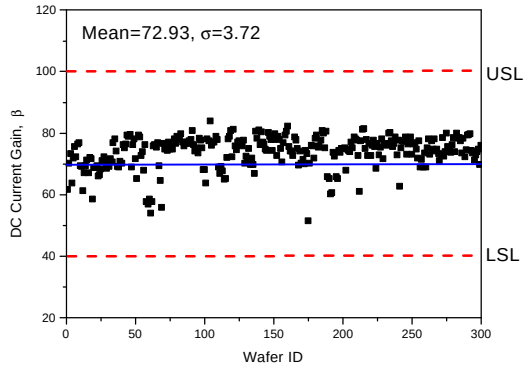

Fig. 3(a). SPC chart of dc current gain (β) for 2μm HBT process. β is measured at J_C=1.25 KA/cm^2.

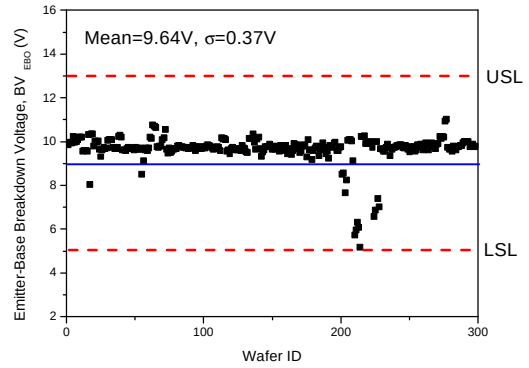

Fig. 3(b). SPC chart of E-B junction breakdown voltage for 2μm HBT process.

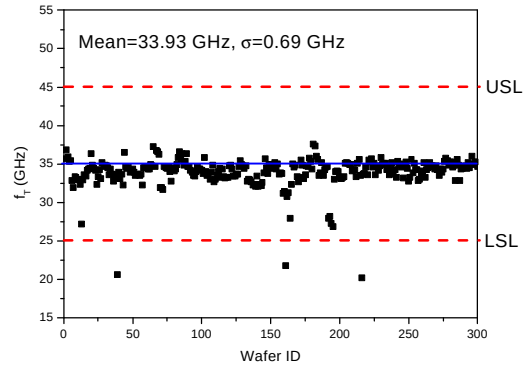

Fig. 3(c). SPC chart of current gain cutoff frequency f_T for 2μm HBT process. F_T is measured at V_{CE}=3.6V and J_C=25KA/cm^2.

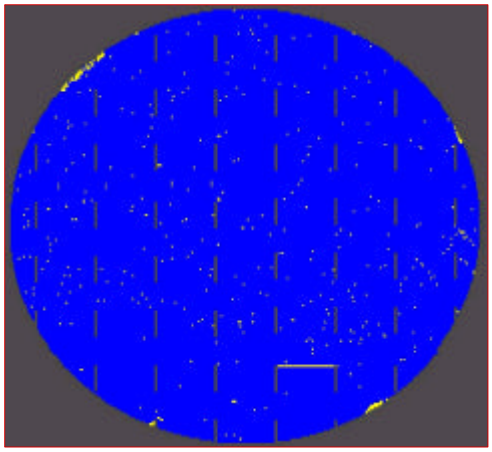

Fig. 4. An example of die yield mapping for HBT power amplifier. Within the 5mm wafer exclusion zone, 469 dies out of 46,853 dies fail (marked with dots).

Parameter Description	Parameter_ID	Unit	Value	
			2μm HBT*	1μm HBT#
Current gain cutoff frequency**	f_T	GHz	35	65
Maximum frequency of oscillation **	f_{max}	GHz	100	80
DC Current Gain (peak)	NA	NA	80	130
Base Sheet Resistence	RS_PW_B2	ohm/sq	180	240
E-B Junction Breakdown Voltage	BK_EB	V	9.8	8
C-B Junction Breakdown Voltage	BK_CB	V	23.8	17
E-C Junction Breakdown Voltage	BK_EC	V	>12	9

* Emitter area 80 μm², # Emitter area 14 μm²
** Test condition: V_{CE}=3.6V and Jc=25KA/cm² for 2μm HBT;
V_{CE} =1.5V and J_C=80KA/cm² for 1μm HBT.

Table 1 Device performance summary for 2μm HBT and 1μm HBT.

Fig. 5 shows the 900MHz loadpull measurement result for a 7680-μm² discrete power cell. The chip is mounted on a test fixture using epoxy. The ground path is conducted from the emitter through via holes to the fixture ground plane. The input and output are wire-bonded to the transmission lines on the fixture carrier. When biased at V_{CE}=3.6V and I_C=300mA (fixed V_{BE}) under CW operation without using harmonic tuning, the discrete power cell is able to deliver 36dBm output power with a peak power-added efficiency (PAE) of 64%. The power density is 1W/mm normalized to the total emitter length or 0.52mW/μm² normalized to the total emitter area.

Fig. 6 shows the 1.85GHz loadpull measurement result for a 7680-μm² discrete power cell. When biased at V_{CE}=3.6V under CW operation using harmonic tuning, the discrete power cell is able to deliver 36dBm output power with a peak power-added efficiency (PAE) of 75%. The chip photograph is shown in Fig. 7.

For lightwave applications at 10Gb/s line rate, a transimpedance amplifier (TIA) and a liming amplifier have been demonstrated using 2μm HBT and 1μm HBT, respectively. Fig. 8 shows the 10Gb/s eye diagram for a limiting amplifier using 1μm HBT process.

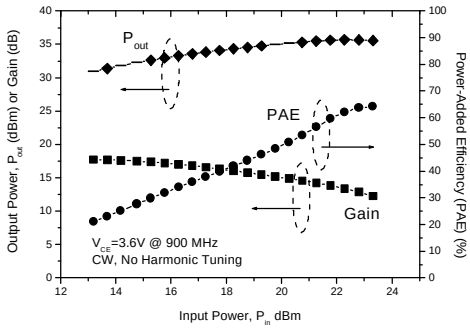

Fig. 5. Loadpull measurement result for a 7680 μm² discrete power cell at 900MHz.

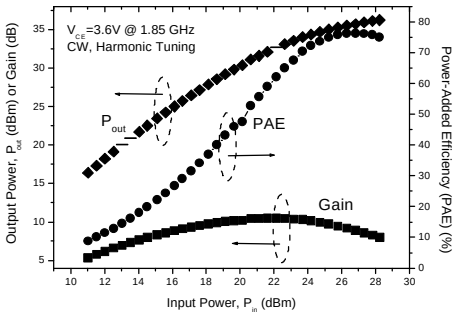

Fig. 6. Loadpull measurement result for a 7680 μm² discrete power cell at 1.85GHz under CW operation with harmonic tuning.

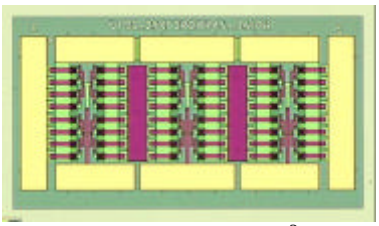

Fig. 7. The photograph of a 7680-μm² discrete power cell without pre-match circuit.

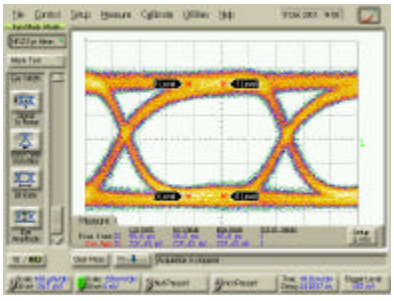

Fig. 8. 10Gb/s eye diagram for a limiting amplifier using 1μm HBT process.

DEVICE RELIABILITY

The relative change in current gain (β) as a function of time for the 2μm HBT technology is shown in Fig. 9. The current gains have been found to be stable during bias stress testing at junction temperature of 259°C (T_a=165°C) with collector current density of 25KA/cm^2 for over 2000 hours (tests are continuing). In order to expedite the acquirement of activation energy, high junction temperatures (337°C, 356°C, and 376°C) are used in the life test. The extrapolated MTTF at a junction temperature of 125 °C is 1×10^9 hours with an activation energy of 1.6 eV, as shown in Fig. 10.

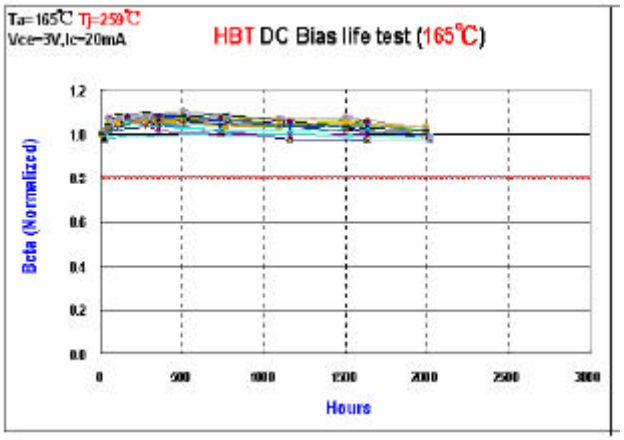

Fig. 9. Bias stress test results at 259 °C junction temperature for 2μm HBT.

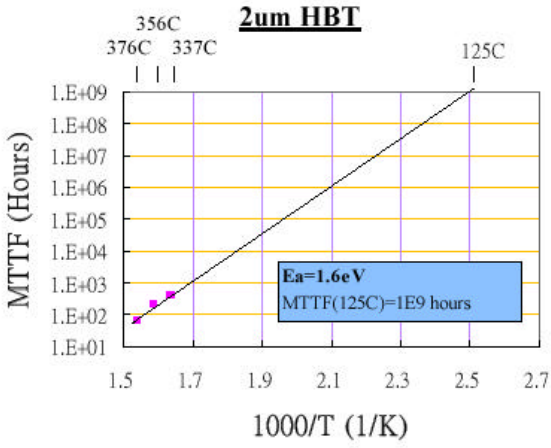

Fig. 10. Three-temperature preliminary life test result for 2μm HBT.

The bias stress test as a function of time for the 1μm HBT technology is shown in Fig. 11. When biased at V_{CE}=3V and J_C=50KA/cm^2, the current gain is stable during bias stress test for over 1800 hours (tests are still continuing). The three-temperature life test is also on going.

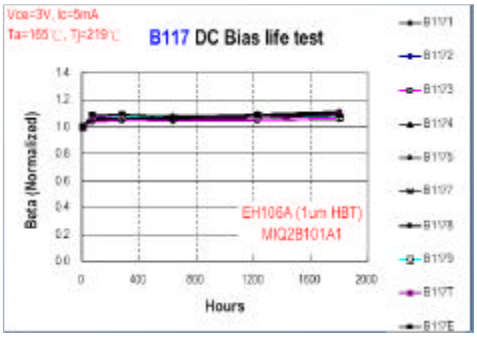

Fig. 11. Bias stress test results at V_{CE}=3V and J_C=50KA/cm^2 for 1μm HBT.

For passive components, thin film resistors and MIM capacitors, high temperature storage test is performed at 280°C for 1000 hours without observing any change in resistance and capacitance. Fig. 12 shows the voltage ramp test result on 3pF MIM capacitors (100μm×100μm) with sample size of 45. Tight MIM capacitor breakdown distribution is measured, indicating good SiN quality and uniformity.

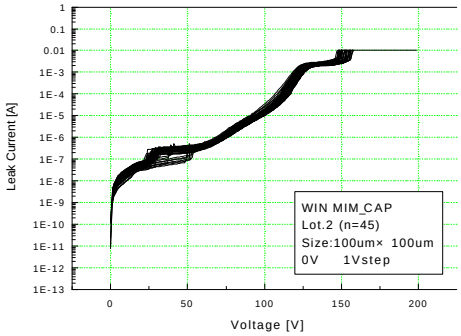

Fig. 12. The voltage ramp test result on 3pF MIM capacitors (100μm× 100μm) with sample size of 45.

CONCLUSIONS

We have demonstrated a high yield InGaP HBT manufacturing technology on 150-mm GaAs substrates. The demonstrated high performance InGaP HBT technology provides a cost effective and reliable solution for various wireless and lightwave communication applications.

REFERENCES

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[2] J. C. C. Fan, *Heterostructure Device Wafer Manufacturing for Telecom Applications for 4" and 6" Wafer Fabs*, 1999 GaAs MANTECH Technical Digest, pp. 193-197, April 1999.
[3] H. C. Chou et al., *Design of Experiments to Achieve High Yield Manufacturing at 6-inch Foundry*, in this Technical Digest.