

Development of Motorola's InGaP HBT Process

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ABSTRACT

This paper reports on the development of InGaP HBT process at Motorola Compound Semiconductor One facility (CS-1) with emphasis on the process critical modules. These modules include: emitter definition by selective wet etches, base contact formation by non dielectric assisted lift-off, collector and isolation selective dry etch, and low parasitic airbridge process. Moreover, device results of both linear and saturated power applications are reported.

INTRODUCTION

InGaP HBT technology delivers high power density, high efficiency, superior linearity, and single supply operation. This makes the InGaP HBT an attractive solution for power amplification in portable wireless applications. Due to the rapidly increasing market share for GaAs HBTs, Motorola developed a third generation InGaP HBT in its Compound Semiconductor One facility (CS-1). Although first and second generation HBT technologies are used in the majority of HBT products, third-generation HBTs (C-doped InGaP/GaAs) offer several acknowledged advantages. InGaP HBTs have superior reliability [1-2] due to the lower initial defect density of InGaP, and its lower defect mobility in comparison to the widely used AlGaAs. In addition because of the minimum conduction band offset between InGaP in the emitter and GaAs in the base, InGaP HBTs have improved uniformity of current gain over current [3] and temperature [4]. Furthermore, the carbon doping in the base prevents the dopant out-diffusion degradation mechanism common to the widely used beryllium doping in AlGaAs HBTs [5].

Besides superior performance and reliability, the InGaP HBT process has superior manufacturability. This paper reports on the process developed at CS-1 with emphasis on robustness of the different process modules.

DEVICE FABRICATION

A cross-section of the InGaP HBT device is shown in figure 1. The fabrication process includes forming a

thermally stable, low resistance, low stress, non-alloyed emitter contact using sputtered TiWN. Subsequently, the emitter and ledge are defined by a series of selective wet etches. The fully depleted ledge reduces recombination currents, thus increasing the current gain, decreasing the noise, and improving the device reliability. A non-alloyed base contact is formed by a single layer lift-off process, resulting in a damage free base surface.

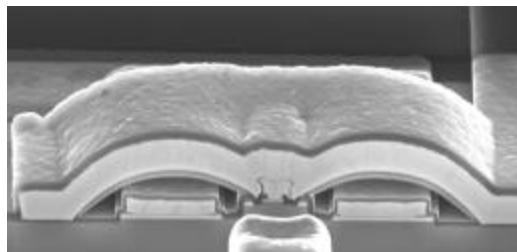


Figure 1. A cross-section of an InGaP HBT

The collector is formed by a highly selective anisotropic self-aligned dry etch. The collector contact is an alloyed NiGeAu formed by a dielectric assisted lift-off process. The devices are isolated by an anisotropic self-aligned dry etch through the subcollector. The rest of the fabrication process involves dielectric deposition and via etching. The process includes two layers of interconnect. Plated Metal1 caps the emitter, base, and collector. Metal2 is a plated airbridge. The airbridge allows managing challenging topography while helping reduce thermal resistance. After connecting all three terminals of the device, a thick nitride layer is deposited for passivation. The wafers then are mounted on sapphire substrates to prepare for the through substrate via etching. This process involves a plasma etch through the GaAs substrate stopping on gold. Gold as back metal is finally plated in the vias.

PROCESS DETAILS

Compound Semiconductor One was converted to 150mm wafer size to increase capacity and meet the high demand for GaAs products [6]. Thus, the current InGaP HBT process is in production on 150mm wafers. The process includes refractory emitter contacts, non-alloyed base contacts, alloyed collector

contacts, a MIM capacitor process, low-parasitic airbridges, and through-wafer vias for minimum ground inductance.

Emitter Definition

The emitter is defined by a series of wet etches. The process involves selectively etching six epitaxial layers and three challenging interfaces.

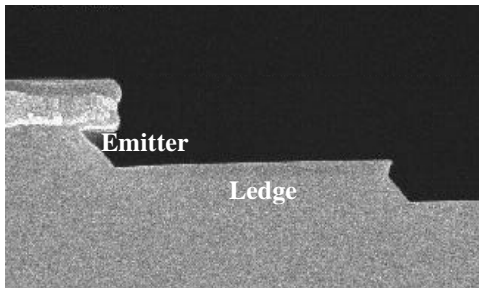


Figure 2. A cross-section of an emitter and ledge.

Sputtered TiWN forms a thermally stable, low resistance, low stress emitter contact. This contact is reliable for high-performance HBTs. Using TiWN as a mask, the emitter epi is selectively etched using a citric acid based chemistry. This etch is very reliable and exhibits a virtually infinite selectivity to InGaP [7].

InGaP etching is more complex and has been one of the major challenges for manufacturing InGaP HBTs. InGaP is difficult to etch due to phosphorous tailing into top layers, thus forming challenging interface layers of non uniform thickness and composition. At CS-1 we have successfully developed a reliable interface etch that selectively removes the interface and stops on InGaP. Another challenge for etching InGaP is making sure it is grown with a high degree of disorder. A specific mixture of Phosphoric:Hydrochloric acid is used to successfully etch InGaP with different degrees of ordering. This chemistry is also highly selective to GaAs, thus resulting in a damage free base surface.

With the selective interface etches and the InGaP etch which is both selective and not sensitive to ordering, the emitter wet etch module guarantees a controllable emitter undercut with a very repeatable ledge thickness, figure 2. Overall, the emitter definition module provides the manufacturability control needed for high volume production.

Due to the complexity of this module, SE (Spectroscopic Ellipsometry) is used as a monitoring technique. SE is a nondestructive method of checking

the thickness and composition of epitaxial layers. In the case of the emitter wet etches, the thickness and composition of the unetched layers are checked using SE after every etch. This method confirms the completion of the etches, and flags any wafers with incomplete etching.

Base Contact Formed by a Single Layer Lift-off

The HBT base contact is a non-alloyed TiPtAu formed on p+ carbon-doped base epi. This contact is formed by a non-dielectric assisted lift-off or single layer lift-off. The base surface is critical to the reliability of the device. Thus using the single layer lift-off prevents damage normally caused by dielectric etches in dielectric assisted lift-off.

Device fabrication is a major part of device intrinsic reliability. In the case of InGaP HBTs, the excellent selectivity of the InGaP etch to the GaAs guarantees a damage free reliable base surface. The wet etch coupled with a single layer lift-off provides a manufacturable process capable of high volume production of reliable devices.

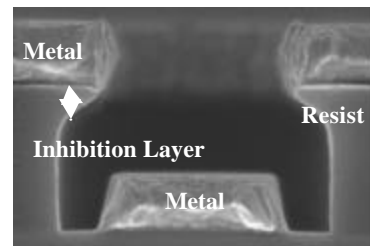


Figure 3. Shows the photoresist profile with the evaporated metal before lift-off.

The single layer lift-off process relies entirely on having the appropriate photoresist profile for a successful lift-off. The profile consists of an inhibition layer that provides the discontinuity in the evaporated metal film as well as controls the base critical dimension, figure 3. The inhibition layer is formed as a result of soaking the top surface of the resist with the developer. The developer is driven to a certain depth after a soft bake. This depth determines the thickness of the inhibition layer. Subsequently, the inhibition layer is defined following exposure and develop due to the slower dissolution rate of the inhibition layer relative to the bulk resist [8].

Collector and Isolation Selective Dry Etch

The collector is defined by a self aligned anisotropic dry etch process. This process dry etches GaAs and selectively stops on AlGaAs. BCl_3 and SF_6 are the active gases used. Fluorine in SF_6 reacts with

Aluminum in AlGaAs to form AlF_3 . AlF_3 has a low vapor pressure, and thus creating an effective etch stop [9].

The etching is done in an Inductive Coupling Plasma (ICP) system at low pressure and temperature. This etch is anisotropic and results in a near vertical damage free surface and sidewall, Figure 4. Both base metal and photoresist are used as etch masks with acceptable selectivity to photoresist and gold.

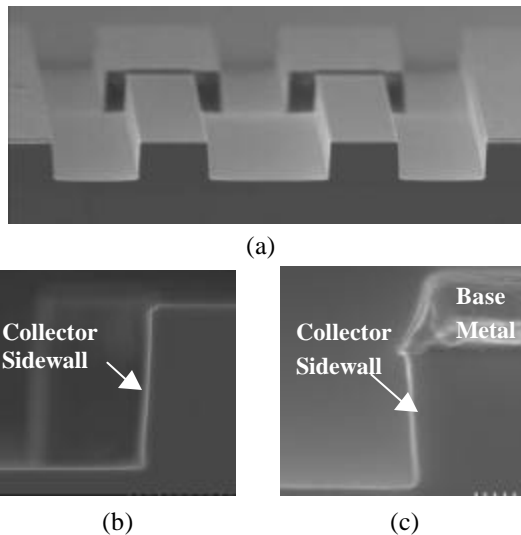


Figure 4. (a) Collector dry etched profile, (b) with photoresist as an etch mask, (c) with base metal as an etch mask.

The photoresist etch rate is $\sim 33\text{\AA}/\text{min}$ and the GaAs etch rate is $\sim 1350\text{\AA}/\text{min}$ with a 30:1 selectivity to AlGaAs. A plot of GaAs and AlGaAs etch rate as a function of time shows the robustness of the process as reflected by selectivity to AlGaAs figure 5.

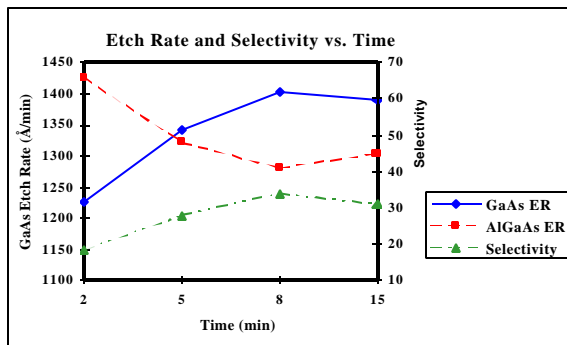


Figure 5. Etch rates and selectivity versus time.

The AlGaAs:GaAs selectivity was also investigated as a function of Aluminum concentration. Acceptable selectivity was found for Aluminum concentration as low as 5%.

This process is also used to define the isolated area by first etching nonselectively through the collector AlGaAs etch stop and then switching to a selective etch process which stops at the AlGaAs etch stop underlying the subcollector.

Airbridge

A low parasitic airbridge process that allows managing challenging topography and helps in reducing thermal resistance is another unique and important part of the process.

The airbridge is formed by first defining a pattern in photoresist which determines the areas under the bridge. This first layer resist is then reflowed to round the corners. Next, a barrier/seed metal layer is sputter deposited. Following the barrier/seed metal deposition, a second layer of photoresist is applied. This layer defines the areas to be gold plated. The wafers are then plated, the second layer of resist stripped, and finally the seed layer is depleted. The barrier metal is then etched exposing the first layer of resist. The first resist layer is stripped thus leaving an airbridge structure. As a final step, the ruggedness of the airbridges is improved by depositing a thick Silicon Nitride. Additionally this passivation layer strengthens the airbridges and prevents scratches and other defects during subsequent processing, packaging and assembly. Figure 6 shows passivated airbridge structures with and without topography.

These airbridged structures have been shown to survive standard CS-1 3-mil backside processing as well as assembly with no apparent damage.

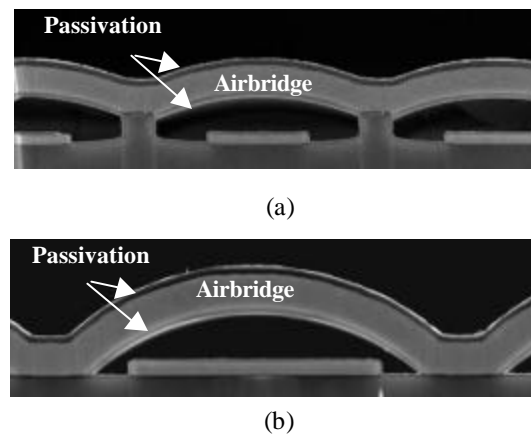


Figure 6. Passivated airbridge, (a) with topography, (b) without topography.

DEVICE RESULTS

Typical device performance shows excellent results for both saturated and linear power applications [10]. For devices using $3 \times 100 \mu\text{m}^2$ emitters, measured at 3.2 V, at an emitter current density of $2.5 \times 10^4 \text{ A/cm}^2$, both f_T and f_{MAX} exceed 40 GHz. Power devices consisting of thirty-six $2 \times 100 \mu\text{m}^2$ emitters ($7200 \mu\text{m}^2$ total emitter area) achieve saturated power > 36dBm with >70% power-added efficiency at 900 MHz, with >10 dB associated gain, Figure 7. Peak power-added efficiency is 72.6 at 36.9dBm. As a linear performance benchmark, a power device consisting of 24 emitters (each $3 \times 80 \mu\text{m}^2$, total emitter area of $5760 \mu\text{m}^2$) achieves 1.95 GHz W-CDMA performance of 28.0dBm output power, ACP= -37.3 dBc, ALT= -48.63 dBc, with 57% power-added efficiency and 10.9 dB associated gain.

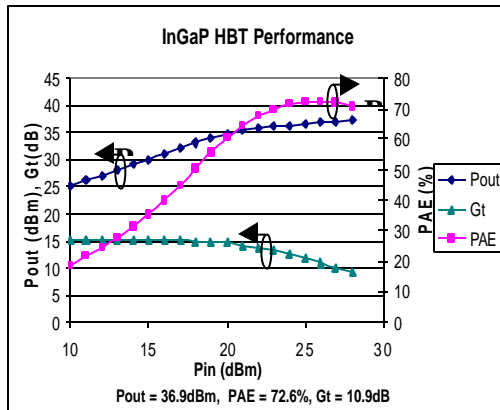


Figure 7. InGaP HBT performance at 900MHz, $V_{ce}=3.2\text{V}$, $I_{cq}=350\text{mA}$.

SUMMARY

An InGaP HBT process was successfully developed at CS-1 on 150mm substrates for high volume production. The robustness and manufacturability of the process are reflected in the emitter definition by selective wet etches, base contact formation by non dielectric assisted lift-off, collector and isolation selective dry etch, and low parasitic airbridge process. Devices show good linear performance as well as excellent efficiency for saturated applications.

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REFERENCES

- [1] T. S. Low, C. P. Hutchinson, P. C. Canfield, T. S. Shirley, R. E. Yeats, J. S. C. Chang, G. K. Essilfie, M. K. Culver, W. C. Whiteley, D. C. D'Avanzo, N. Pan, J. Elliot, and C. Lutz, "Migration from an AlGaAs to an InGaP emitter HBT IC process for improved reliability," *1998 GaAs IC Symposium Technical Digest*, pp. 153-156.
- [2] A. Gupta, A. Young, and B. Bayraktaroglu, "InGaP makes HBT reliability an non-issue," *2001 GaAs MANTECH Technical Digest*, pp. 203-206.
- [3] T. Henderson, "Physics of degradation in GaAs-based heterojunction bipolar transistors," *Microelectronics Reliability* **39**, pp. 1033-1042 (1999).
- [4] W. Liu and S.K. Fan, "Near-ideal I-V characteristics of GaInP/GaAs heterojunction bipolar transistors," *IEEE Electron Dev. Lett.* **13**, pp. 510-512 (1992).
- [5] D. Hill and J. Parsey, "Interaction of degradation mechanisms in Be-doped GaAs HBTs," *2000 IEEE GaAs IC Symposium Technical Digest*, pp. 241-244.
- [6] M.R. Wilson, K. Adams, and E. Huang, "Riding the Wireless Wave With 150mm GaAs Manufacturing," *2000 GaAs MANTECH Technical Digest*, pp. 245-248.
- [7] A. Hanson, D. Danzilio, K. Bacher, and L. Leung, "A selective gate recess process utilizing MBE-grown InGaP etch-stop layers for GaAs-based FET technologies," *IEEE Electronic Device Letters*, pp.195-197, 1998
- [8] R. Redd, D. Maurer, and L. S. Klingbeil, "Revitalization of Single Layer Lift-off for finer resolution and challenging topography," *2001 GaAs MANTECH Technical Digest*, pp. 99-101.
- [9] S. J. Pearton, F. Ren, T. R. Fullowan, A. Katz, S. Hobson, U. K. Chakrabarti, and C. R. Abernathy, "Plasma etching of III-V semiconductor thin films," *Materials Chemistry and Physics*, **32**, pp. 215-234, 1992.
- [10] P. Savary, A. Girardot, G. Montoriol, F. Dupis, B. Thibaud, R. Jaoui, L. Chapoux, V. Esnault, L. Cornibert, O. Izumi, D. Hill, M. Sadaka, H. Henry, E. Yu, M. Tutt, M. Majerus, R. Uscola, F. Clayton, C. Rampley, S. Klingbeil, K. Rajagopalan, A. Mitra, A. Reyes, "Dual-Band multi-mode power amplifier module using a third generation HBT technology," *2001 IEEE GaAs IC Symposium Technical Digest*, pp. 71-74.