GaAs-Based Heterostructures on Silicon

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Abstract

The combination of the superior electrical and optical performance of III-V semiconductors with mature silicon technology has been very attractive for the semiconductor industry. The successful integration of the III-V compound semiconductors with silicon opens the door to many advanced electronic and optoelectronic applications.

We review the recent progress on epitaxial heterostructures of oxides and GaAs-based compound semiconductors on silicon. Device quality GaAs-based heterostructures have been grown on Si substrates up to 200mm and 300mm in diameter by molecular beam epitaxy (MBE) at Motorola Labs and IQE, respectively. An epitaxial $SrTiO_3$ (STO) layer and an amorphous interfacial layer are used as a combined buffer layer between the compound semiconductor and Si substrate. Field effect transistors (FETs) fabricated in the GaAs epi-layers show performance comparable to similar devices fabricated on GaAs substrates. The mobility in the GaAs/STO/Si sample is 2,524 cm^2/V-s compared to a GaAs/GaAs sample with mobility of 2,682 cm^2/V-s. A 0.7 mm gate length device has I_{dmax} of 367 mA/mm and G_{mmax} of 223 mS/mm. These devices also have good RF performance with f_{max} of 14.5 GHz and class A power density in a 3mm device of 90 mW/mm with an associated power added efficiency of 38%. This RF performance is within experimental error of similar devices fabricated on GaAs substrates. Lifetime of these devices was also measured. After 800 hours at 200 °C, the GaAs/STO/Si sample showed 1.2% degradation in drain current.

INTRODUCTION

The combination of the superior electrical and optical performance of III-V semiconductors with mature silicon technology has been very attractive for the semiconductor industry. The successful integration of the III-V compound semiconductors with silicon reduces substrate and processing cost for III-V compound semiconductor manufacturing. It opens the door to significantly less expensive optical communications, high-frequency radio devices and high-speed microprocessor-based subsystems by potentially eliminating the current cost barriers holding back many advanced applications.

For many years, most attempts to grow device quality GaAs-based heterostructures on Si[1-6] have not proven commercially successful. This is mainly due to the considerable lattice and thermal expansion coefficient mismatch between GaAs and Si which has led to high misfit dislocation densities, inferior performance and poor reliability in the GaAs/Si devices. In this presentation, we review the recent progress on GaAs-based heterostructures grown on large size Si substrates by MBE at Motorola Labs and IQE. A unique STO/SiO_2 stack buffer layer inserted between GaAs and Si substrate has been used to form device quality GaAs/STO/Si heterostructures. Materials properties and device performance of the GaAs/STO/Si heterostructures are very similar to the GaAs/GaAs control samples in all aspects. Threading dislocation defect density as low as $5x10^4$ defects/cm^2 and electron mobility as high as 94% of GaAs/GaAs control samples have been obtained for a ~2 µm thick GaAs film on Si. Well-behaved MESFETs have been fabricated and tested. Device RF performance and reliability have also been studied.

EXPERIMENTAL

1) STO growth on Si: The growth process started with commercial prime Si wafers up to 300mm in diameter. Production-type MBE systems were used to deposit STO thin films on Si substrates. Sr and Ti metals were evaporated using effusion cells and molecular O_2 was introduced into the growth chamber in a controlled fashion. Substrate temperature and chamber pressure during oxide growth were 300-700°C and up to 10^{-5} mBar, respectively. RHEED technique was used to calibrate the metal fluxes and to monitor the growing surface in real time. Two-dimensional STO growth as evidenced by persistent RHEED intensity oscillations is achieved and AFM rms roughness of 0.2nm is obtained for a 13nm thick STO film. XRD and HRTEM measurements indicate that the STO films are

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crystalline and a SiO_2 interfacial layer exists between STO and Si.

2) GaAs heteroepitaxy: After STO deposition, the STO/Si wafers were transferred to a production-type III-V MBE chamber. A Ga effusion cell and an As valved cracker were used for GaAs growth. Si from an effusion cell was used as an n-type dopant. Standard Hall and MESFET structures were grown on the STO buffered Si substrates in the III-V MBE chamber. A thin GaAs seed layer was first grown on the STO buffered Si substrate. An undoped GaAs buffer layer is then grown on top this initial GaAs seed layer to electrically isolate the active GaAs devices from the Si substrate. As a comparison the MESFET structure was grown simultaneously on a GaAs substrate. Material properties from consecutive runs are compared to demonstrate repeatability.

50nm n+GaAs Cap
150nm n GaAs Channel
2µm GaAs Buffer
5nm $SrTiO_3$
2nm SiO_2
Si Substrate

Fig. 1 GaAs MESFET Structure on Si

3) MESFET fabrication: As a first demonstration of the device potential for this technology, a GaAs MESFET has been fabricated. Schematically shown in Fig. 1, the device consists of a 150nm channel doped with $8x10^{17}/cm^3$ and a 50nm contact layer doped at $5x10^{18}/cm^3$ grown on top of a 2µm GaAs buffer layer. For comparison, identical MESFET structures were also grown on normal GaAs control wafers. Devices were then fabricated on these samples using standard MESFET processing techniques. Device isolation was achieved through the wet etching of a mesa. Ni/Ge/Au ohmic contacts were then deposited and patterned by liftoff and annealed by RTA to form ohmic contacts to the n+ cap. A wet gate recess was used to etch the cap in the gate region, then the Ti/Pt/Au gate was deposited by e-beam evaporation and lifted off using optically defined photoresist patterns. The process used on the GaAs/STO/Si sample was identical to the process used to fabricate the GaAs/GaAs sample. FatFETs with gate lengths of 20 µm were used to characterize the electron mobility.

RESULTS AND DISCUSSION

1) Physical properties: Very sharp RHEED streaks with Kikuchi lines and Laue zone diffractions are observed for GaAs/STO/Si suggesting very smooth and highly ordered GaAs surface. The surface morphology is excellent and mirror-like. AFM measurements confirm that the rms roughness is about 0.9 nm over a 10x10 μm^2 area. Both RHEED and AFM also suggest that the GaAs films grown on STO/Si are single-domain.

Fig. 2 shows an XRD spectrum of a GaAs/STO/Si sample. It clearly indicate that the GaAs film is single crystalline. Pole figure XRD measurements together with the RHEED observation establish that the GaAs unit cell aligns with that of the Si substrate.

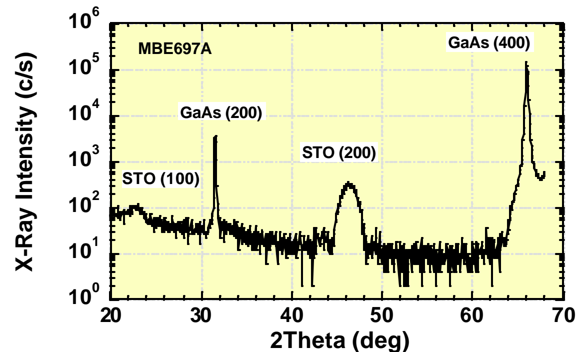

Fig. 2 XRD spectrum of a GaAs/STO/Si heterostructure.

Fig. 3 is the cross-sectional HRTEM picture of a GaAs/STO/Si heterostructure. An amorphous SiO_2 layer is also clearly seen between STO and Si.

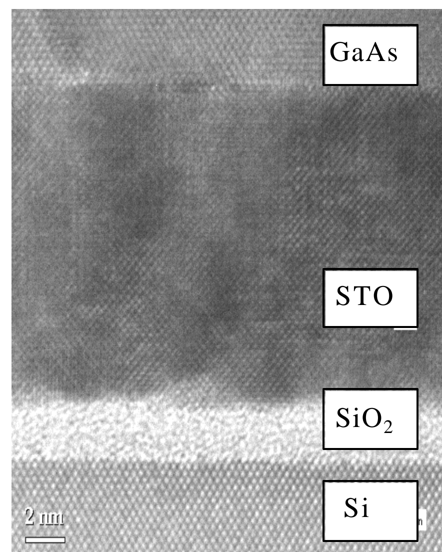

Fig. 3 HRTEM micrograph of GaAs/STO/Si.

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By using A/B etch of the top GaAs layer, an EPD of $5x10^4$ cm^{-2} is obtained for a ~2µm GaAs film grown on Si using STO/SiO_2 buffer layer. This is comparable to a commercial GaAs LEC wafer measured with the same technique[7].

2) Hall mobility and device characteristics: Hall mobility measurements on GaAs/STO/Si heterostructures show an electron mobility of 2,524 cm^2/V-s compared to a GaAs/GaAs sample with mobility of 2,682 cm^2/V-s, i.e., the mobility reaches 94% of the control GaAs sample. Repeatability of Hall mobility over 90% of the controls is demonstrated for consecutive GaAs/STO/Si runs

Drain current–drain voltage curves are shown in Fig. 4 for the GaAs/STO/Si 0.7µm x 100µm MESFETs and the GaAs control samples. The saturation current at 0.5V forward gate bias is 367 mA/mm and 385 mA/mm for the GaAs/STO/Si and the GaAs samples, respectively. The maximum transconductance is 223 mS/mm and 240 mS/mm for the GaAs/STO/Si and the GaAs control samples respectively. The gate diode characteristics for devices again show no significant difference between the samples with both having forward turn-on voltages of 0.6V and reverse breakdown voltage difference less than 5%.

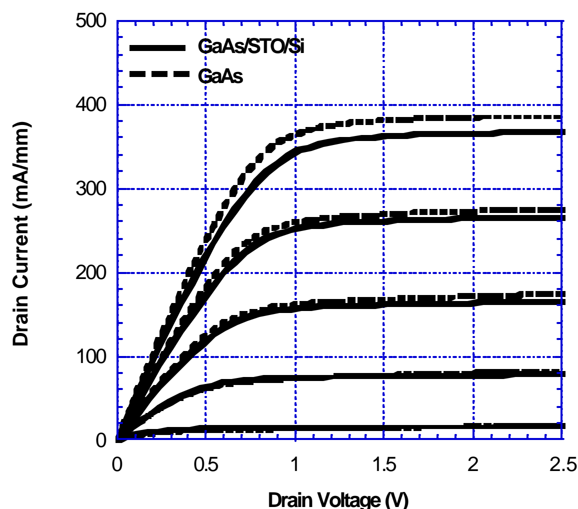

Fig. 4 Drain current–drain voltage characteristics for 0.7µm x 100µm GaAs/STO/Si MESFETs. Gate voltage maximum is 0.5V and gate voltage step size is 0.5V.

RF characteristics were measured on-wafer using ground-signal-ground probes. The devices are all biased with V_{ds} = 3.5V. The maximum available gain of the GaAs/STO/Si devices compares very favorably with the GaAs devices. Maximum stable gain of about 18dB was demonstrated for the GaAs/STO/Si 0.7µm x 3mm devices. f_{max} of these devices is about 14.5 GHz, which is within the window demonstrated for these devices on a standard GaAs substrate. Differences between the GaAs devices and the GaAs/STO/Si devices are within process variation.

Large signal performance was evaluated next using on-wafer load-pull techniques. The 0.7µm x 3mm device was measured at 1.9GHz and matched for maximum output power. The GaAs/STO/Si device was biased near Class A at V_{ds} = 3.5V and I_{ds} = 207mA. The well-behaved compression curve shows 18.6dB maximum gain and 24.28dBm of output power at the 1dB compression point, which represents a power density of approximately 90 mW/mm. The associated power added efficiency for this device was 38%. The GaAs/GaAs device matched for maximum output power under the same bias conditions also had a power density of 90 mW/mm with an associated power added efficiency of 40%.

Of primary importance in any GaAs/Si device is its reliability. Initial lifetime measurements have been carried out on both the GaAs/STO/Si sample and the GaAs/GaAs sample. For this measurement 0.7µm x 100µm devices from both samples were used. After a burn-in period, both devices were placed on a hot chuck set at 200 °C and biased at 3.5V V_{ds} and –0.5V V_{gs}. Both the GaAs/STO/Si devices and the GaAs/GaAs devices exhibit an initial slow degradation. At longer times the GaAs/GaAs sample went into a secondary degradation mode and reached 10% degradation at 450 hours. The GaAs/STO/Si sample has currently been measured up to 800 hours and remains at about 1.2% degradation.

CONCLUSIONS

Device quality GaAs-based heterostructures have been grown on Si substrates up to 300mm in diameter by using MBE at Motorola Labs and IQE. Materials properties and device performance of the GaAs/STO/Si heterostructures are very similar to the GaAs/GaAs control samples in all aspects. This technology opens the door for the integration of GaAs-based devices with Si technology for many advanced applications.

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ACRONYMS

MBE: Molecular Beam Epitaxy
RHEED: Reflection High Energy Electron Diffraction
AFM: Atomic Force Microscopy
XRD: X-Ray Diffraction

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HRTEM: High Resolution Transmission Electron Microscopy
MESFET: Metal Semiconductor Field Effect Transistor
EPD: Etch Pit Density
RF: Radio Frequency