GaAs and SiGeC BiCMOS Cost Comparison – Is SiGeC Always Cheaper?

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Abstract

GaAs has enjoyed a relatively unchallenged position as the RF semiconductor material of choice for many RF applications at or above 1GHz, but particularly in RF front-end sockets for cellular telephones. But, over the past several years SiGeC BiCMOS technology has pushed GaAs out of many of these sockets due to it's high performance, high level of integration, and low cost attributes. Will this trend continue to the power amplifier? Is this technology really cheaper to develop and manufacture RF product solutions than GaAs? Is SiGeC really the RF technology of the future, or only a short-lived fad to be pushed aside by RF CMOS? This paper will explore the driving factors behind these questions, and moreover, explore the product entry and manufacturing cost differences for GaAs HBT, and SiGeC BiCMOS technology.

INTRODUCTION

For the past 25 years GaAs has struggled to achieve the status of a mainstream RF semiconductor technology. The relatively high cost of substrate materials, the slow pace to large diameter manufacturing, and the relatively small scale of manufacturing operations has compounded this struggle relative to its Si counterparts. Despite these issues, GaAs has achieved wide acceptance in the RF front end of almost every cellular phone on the market today, particularly in the power amplifier socket as a result of its outstanding RF characteristics [1,2].

However, over the past several years GaAs has seen its presence as an RF semiconductor technology for wireless handheld device sockets such as LNA's, mixers, and even power amplifiers being challenged and supplanted by SiGeC HBT technology [3,4]. This is particularly true on the receive side of radios operating at frequencies from 1 to 5 GHz. A typical cellular telephone block diagram is shown in Figure 1 with the most common semiconductor technology choice shown for each major radio sub-section. The transceiver is almost exclusively realized in SiGeC BiCMOS today because of the technology's ability to simultaneously deliver excellent RF performance, high levels of integration, and low power dissipation at very reasonable costs. Ironically, the push toward higher integration RF modules is opening the door for SiGeC technology to enter the transmit side of the radio. Today's transmit modules offer the flexibility to cost effectively combine multiple semiconductor technologies to realize the most cost effective RF solutions. This may result in the some portions of the power amplifiers being migrated onto a SiGeC IC within the module. This paper will explore the driving factors behind these trends, and explore the product entry and manufacturing cost differences between GaAs HBT, and SiGeC BiCMOS technology.

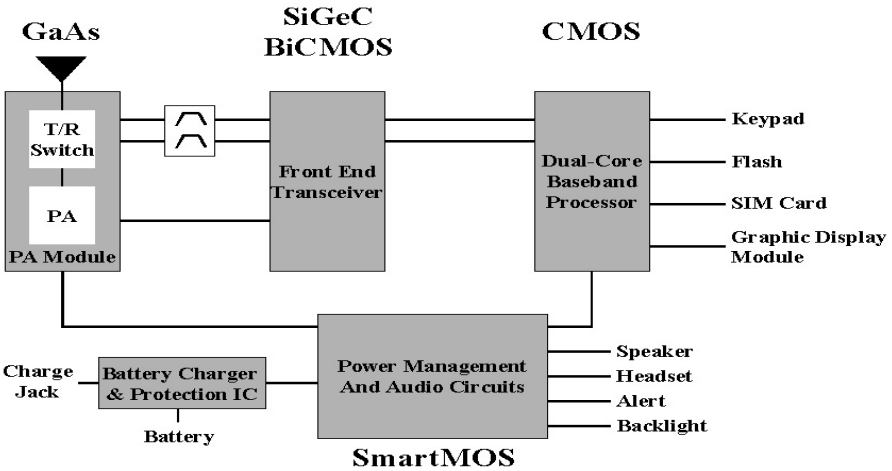

Figure 1. Semiconductor technology partitioning choices for major sub-sections of Motorola's i.250 Innovative Convergence Platform solution for 2.5G GSM/GPRS phones.

TECHNOLOGY PERFORMANCE TRADEOFFS

Before discussing the cost tradeoffs of any given set of semiconductor technologies it is important to understand the relative performance advantages and limitations of those technologies. While there is significant publicity in the news media, and even technical journals on which company and technology have demonstrated the highest f_τ (in many cases quoted as the fastest transistor), this is clearly not enough to ensure success in every high frequency application.

Many technology and device attributes play a significant role in determining the best technology choice for a given application. While it is not the purpose of this paper to explore the design tradeoffs for various technologies and applications, it is important to mention a few of the considerations such as transistor f_τ, breakdown voltage device ruggedness, noise characteristics, and the ability to integrate RF passives, etc. to mention just a few. While it is often unmentioned, one of the most significant tradeoffs that dictate the technology choice in certain applications is the relationship between device f_τ and breakdown voltage.

Many applications require not only high operating frequency, but also a simultaneously large voltage swing such as in cellular power amplifiers and 40GB/s fiber optic laser drivers. So, to properly access the applicability of a given high frequency semiconductor technology it is often more important to consider peak f_τ as a function of device breakdown voltage as shown in Figure 2. This figure clearly shows that it is difficult to address high frequency, large voltage swing applications with SiGeC BiCMOS due to the relatively low breakdown voltage, particularly for very high f_τ devices. As stated previously, there are many other application considerations such as the need for large digital content that greatly favor SiGeC. Table I provides a relative

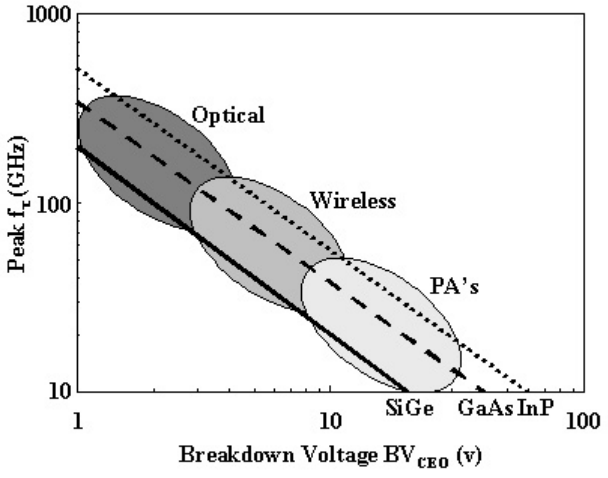

Figure 2. Plot showing f_τ vs breakdown voltage for HBT devices in SiGeC, GaAs, and InP technologies.

Table I
Relative Comparison of Application and Design Tradeoffs for GaAs and SiGeC Technology [4]

Characteritic	GaAs HBT	SiGeC BiCMOS 0.35µm	SiGeC BiCMOS 0.18µm
Active Device			
Beta	100	120	440
f_τ (GHz)	40	50	120
BV_{CEO} (v)	10	3.4	1.9
nf_{min} (1.8GHz)	1.6	0.7	0.3
J_c @ peak f_τ/f_{max} ($mA/\mu m^2$)	0.5	1.5	4.0
Minimum W_e (µm)	2.0	0.4	0.25
Digital Density ($gates/mm^2$)	<1K	18K	100K
Passives			
MIM Cap Density ($fF/\mu m^2$)	1.3	1.6	1.6
Inductor Q (3nH@1.8GHz)	15	20	20
Technology			
Backside Process	Yes	No	No
Levels of Metal	2 to 3	3 to 4	3 to 5

comparison between some of the application considerations for GaAs and SiGeC technologies. *It is important to understand that this comparison is intended to outline important characteristics, and not provide an absolute comparison since the various technologies were not necessarily optimized to compete for the same application.*

MANUFACTURING COST CONSIDERATIONS

Once it is determined which semiconductor technologies can adequately address a specific application, the final choice almost always comes down to cost. To be certain, ***cost*** comes in many forms depending on the potential volume of the targeted application. These include costs from design, photo mask manufacturing, wafer manufacturing, test, and packaging. The up front costs of design turns and photo mask costs can be a very significant impact to final product cost in low volume applications. This paper will primarily focus on the two manufacturing costs, namely photo mask costs, and wafer fabrication cost.

Typical GaAs manufacturing processes use 8 to 16 photo mask layers (depending on metal layers, passive options, etc.) with only one layer typically requiring critical dimensional control. The majority of the layers would use 5", 5X stepper reticles with pellicles. This is contrasted with SiGeC BiCMOS processes that typically require 26 to 36 mask layers with several layers potentially requiring optical proximity correction, and even phase shift technology in some cases. Moreover, the newer steppers often employed in BiCMOS process flows typically require 6", 5X stepper reticles. These differences in photo mask layers, minimum feature size, and reticle size can result in a very significant

Table 2
Typical 5X Photomask Layers, Features, and Costs for GaAs HBT and SiGeC BiCMOS Technologies

Characteristic	GaAs	SiGeC BiCMOS 0.35µm	SiGeC BiCMOS 0.18µm
Typ Min CD (µm)	1.0	0.4	0.2
Layers CD < 0.5µm	0	7	25
Layers With OPC	0	0	7
Phase Shift Layers	0	0	0
Number of Layers	11	27	33
Typical Reticle Size	5"	5" & 6"	6"
Mask Set Cost	$18K	$100K	$180K

cost difference for an engineering or production mask set between GaAs and SiGeC BiCMOS as shown in Table 2.

It is easy to understand that this photo mask cost difference, of greater than $150K in some cases, forms a large barrier to entry when considering low volume designs in SiGeC technology. This is even further exacerbated when the likelihood of multiple design turns is considered. In the case of high volume products the one time costs for masks is much less of a concern since it can be spread over many more finished goods.

The manufacturing cost of any semiconductor wafer is directly related to five major factors, namely: 1) the cost of the starting substrate, 2) the variable costs associated with labor, chemicals, gases, process tool maintenance, etc., 3) the fixed costs from asset depreciation and overhead, 4) total factory wafer volume, and 5) technology process yield. These components can be directly tied to manufactured wafer cost over a given period of time by the following simple equation:

$$\text{Wafer Cost} = \frac{\left[\text{Substrate Cost} + \text{Process Stages For Technology} \bullet \frac{[\text{Total Variable Expenses} + \text{Total Fixed Expenses}]}{\text{Total Process Stages Run In The Factory}}\right]}{\text{Technology Process Yield}}$$

The process stages represent the number of major process blocks that are required to produce a given type of technology. In the simplest form the number of stages could represent the number of mask layers for the technology. This concept is included to more accurately express wafer cost in factories that are running multiple technologies of significantly different process lengths.

Given this relationship, we can explore the potential differences in manufacturing costs between GaAs and BiCMOS technologies. The substrate cost is an obvious place to start. GaAs epitaxial wafers average about $700 per 150mm wafer. This compares to the starting substrate for a SiGeC process that is about $50 per 200mm wafer. When the wafer size is taken into account, it is clear that the GaAs epi wafer cost is 25X more expensive then Si on an area basis. This fact is even more significant when it is realized that the GaAs epi wafer approaches 50% of the total finished wafer manufacturing cost! While there has been significant progress in the past several years, compound semiconductor epitaxial wafer cost is still a major obstacle to competing with Si manufacturing cost.

To 1st order, the variable cost to process a single stage should be quite similar for a GaAs wafer vs a SiGeC wafer. In other words, it would seem reasonable that the cost to deposit an oxide layer, metal layer, or process a photo layer should be similar in terms of labor, chemicals, and gases. However, there are 2nd order effects that benefit a high volume Si factory in terms of full automation, labor, and pooled qualification costs across the larger volume of wafers run in such a factory. Moreover, the machine throughputs, particularly for processes that require temperatures greater than 250 °C, are often substantially reduced for GaAs to prevent thermal stress breakage resulting from GaAs's poorer thermal conductivity, and greater fragility. These throughput differences are outlined in Table 3. In many cases this results in a higher cost per stage to process a GaAs wafer. Lastly, a very large Si factory has the benefit to pool spare parts and maintenance costs across a much larger equipment base. This again has the effect of reducing the cost per processed wafer for SiGeC compared to a smaller scale GaAs factory.

The issue of fixed expenses requires careful consideration. There is no question that the total dollar investment in a typical GaAs factory is at least 5X lower than for a typical 200mm Si factory. However, the impact of full automation and the benefit of very large scale cannot be overstated. The 5X greater investment could easily result in a 10X greater capacity capability. Moreover, the ability to mix several types of Si technologies in the same factory (CMOS, BiCMOS, SiGeC BiCMOS, etc.) greatly improves the probability of keeping the facility effectively loaded, and improves the overall operating efficiency of the factory. The wafer manufacturing cost advantage for SiGeC can be summed up in a few words: *"volume is king"*!

HOW RF CMOS CHANGES THE LANDSCAPE

As 300mm, 90nm CMOS technology comes to center stage in the semiconductor arena over the next five years the

Table 3
Process Tool Throughput Comparisons for GaAs and Si Resulting From Differences In Thermal Conductivity, Material Fragility, and Tool Vintage

Process Tool	Throughput (Wafers/Hour) GaAs (6")	Silicon (8")
Etch (5K Oxide)	20	30
Implant (Average Dose)	40	70
PECVD (2000Å Oxide)	20	57
Photo Aligns	30	35
PVD (Seed Metal)	23	34

technology partitioning choices for wireless devices is sure to change. This technology can yield superb analog and RF capabilities when coupled with a full suite of RF passives that have been honed over several generations of SiGeC technology, and boasts raw digital packing densities approaching 500K gates/mm^2. As an example, NMOS transistors with single gate oxide from this technology have at f_τ of 115GHz at an operating voltage of 1.2v.

CMOS technology will be a strong contender for transceiver designs over the next five years. In fact, it is quite likely that SoC solutions combining the transceiver together with the baseband processor will be realized in advanced RF CMOS technology nodes in the near future. Clearly, RF CMOS can't address any PA functions due to the severe breakdown voltage requirements of the PA. So, ironically the drive to CMOS SoC solutions may actually push SiGeC technology out of the cell phone of the future!

SUMMARY AND CONCLUSION

The semiconductor partitioning choices for any given application is influenced by many factors including, technology capability, cost of design entry, and product manufacturing cost. In the modern cell phone a battle line has formed in the RF front end between GaAs and SiGeC technologies. While GaAs has a stronghold on the power amplifier module (including the RF switches) for the foreseeable future, SiGeC BiCMOS technology has attacked and conquered almost every other RF socket in the cellular phone that was previously occupied by GaAs. The ability of SiGeC BiCMOS technology to push GaAs from these sockets has been driven by it simultaneous ability to deliver compelling RF functions integrated with substantial digital content at very reasonable costs.

The ability to produce SiGeC BiCMOS solutions, particularly high volume solutions, more cheaply than GaAs arises from three major factors: a) 25X cheaper substrate cost for BiCMOS than for GaAs, b) reduced wafer manufacturing cost resulting from very large scale manufacturing centers with superior throughput per capital dollar spent, and c) Si manufacturing is currently at 200mm and moving toward 300mm while GaAs is just moving to 150mm.

While this scenario seems ominous for GaAs, the picture is not really too bleak. GaAs has a solidly earned position in the PA of tomorrow. The trend toward Front End Modules (FEM's) for the PA and their inherent ability to combine semiconductor technologies could mean that GaAs will need to share portions of the PA socket with SiGeC. On the other hand, SiGeC technology is already focused clearly in the gun sights of RF CMOS on the receive side of the radio. The drive toward SoC CMOS solutions may leave no place for SiGeC in the receiver.

The conference presentation will explore the details of the manufacturing cost differences between GaAs HBT and SiGeC BiCMOS wafer manufacturing.

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ACRONYMS

OPC – Optical Proximity Correction
SoC – System on a Chip

