New Manufacturing Concepts for Ultra-Thin Silicon and Gallium Arsenide Substrates

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Abstract

The paper reports on new manufacturing concepts for handling and processing of thin semiconductor substrates. Technologies which were formerly demonstrated for silicon wafers were recently transferred to GaAs substrates and are presented in this paper. As a result of the development work the feasibility for preparing 20 µm thin GaAs wafers showing mechanical flexibility is proven. Due to the application of "Dicing-by-Thinning" concept micro defects at the edges of ultra thin GaAs chips are practically eliminated.
Furthermore a new wafer support technique is proposed: "Smart Carriers" use electrostatically activated carrier plates for temporary bonding of device and support substrates. Their first applications for handling and processing of thin GaAs wafers are presented in the paper.

INTRODUCTION

Within the last years backside thinning of fully processed product wafers has become a widely used technique in semiconductors industry. Steadily increasing demands for extremely low package height in the case of chip card ICs and the requirement for increased electrical performance of power semiconductors and high frequency devices are strong driving forces for the development of thin wafer technology. Fabrication of wafers in the thickness range of less than 100 µm leads to challenging tasks for secure handling and processing of fragile substrates and single dies.

Ultra thin GaAs is a powerful material leading to high end products in the field of communication electronics or optoelectronics respectively. The main objectives in GaAs technology are to evade the poor thermal conductivity and to eliminate long via holes through the substrate for electrical interconnection to the chip backside. Ultra thin GaAs chips allow increased thermal dissipation, simplify vertical interconnection and improve the electrical parameters of the device through the elimination of parasitic elements.

THINNING AND DICING OF SILICON AND GALLIUM ARSENIDE WAFERS

Research work at Fraunhofer Institute IZM is focused on the development of new processing and handling techniques by means of reversibly mounted carrier substrates and the analysis of material strength of thin single chips [1]. It turned out that dicing of a thin wafer has major influence on fracture force and bending behaviour of thinned semiconductor substrates [2]. Best mechanical properties of ultra thin silicon samples were accomplished by applying the technological concept "Dicing-by-Thinning" ("DbyT").

1) The "Dicing-by-Thinning" ("DbyT") concept: According to the "DbyT"–concept trenches are prepared with explicit depths by means of a wafer saw, or more favorable by dry etching techniques, at the front side of a device wafer. Afterwards the wafer is temporarily fixed on a carrier substrate.

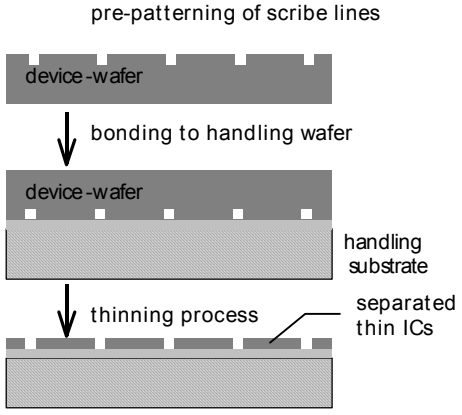

Figure1: Schematic process flow of the "Dicing-by-Thinning" concept for preparation of ultra thin semiconductor devices.

Chip separation takes place during backside thinning when finally the front side grooves are opened. If the last step is a backside spin etching process grooves are rounded by the etchant and possible residual micro-cracks are removed. The etchant serves furthermore as stress relief.

2) Dicing-by-Thinning for silicon wafers: The concept is perfectly suited for small die sizes, e. g. transponder ICs for contactless smart cards. Due to the possibility to reduce the width of dicing lines from 100 µm to 10 µm for dry etched

trenches, the amount of chips per wafer can be strongly increased.

The power of the "DbyT"-method is demonstrated in figure 2: a silicon "e-cube" having edge dimensions of 30 x 30 x 35 μm^3 was prepared. In this case chip separation grooves were prepared by plasma dry etching. It is assumed that such tiny silicon objects, further equipped with IC structures, could become interesting for future self-assembly techniques.

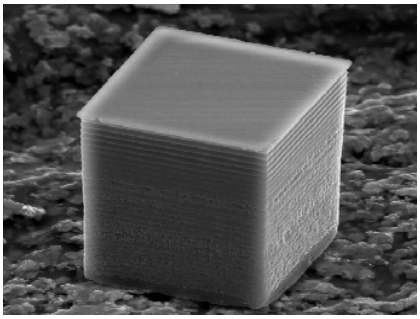

Figure 2: Silicon "e-cube" (dimensions: 30 x 30 x 35 μm^3) prepared according to "Dicing-by-Thinning" concept.

3) Thinning of gallium arsenide wafers: a commercial available GaAs wafer (100) with an original thickness of 100 µm was temporarily fixed onto a carrier substrate by the aid of a temperature releasable tape. Such tapes are coated with two different polymeric adhesives: one permanently adhesive side and one heat-removable side. Subsequently the GaAs stack was thinned by a standard spin-etch process. As backside spin etching medium we took H_2O_2 (30%) / H_2SO_4 (96%) (1:1) at a temperature of 65°C. Chemical etching by use of this system gives high quality GaAs surfaces of low index orientations except for the GaAs [111] surface. Also a medium containing HF (40%) / HNO_3 (65%) / CH_3COOH (100%) / H_2O (1:3:2,3:2,5) at room temperature prepares high quality mirror like surfaces. As further advantage such an etching system does not degrade typical contact metallizations compared to phosphoric etching systems [5].

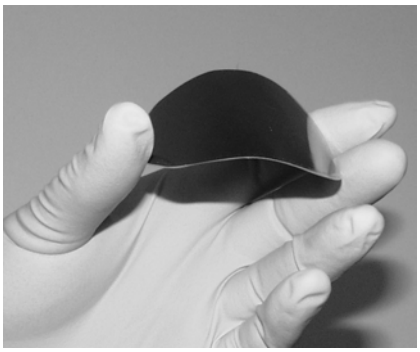

Figure 3: Pliable GaAs wafer, 25 µm thickness, diameter: 3 inches; wafer is laminated onto tape.

The processed GaAs wafer was removed from the carrier substrate with a peel-off temperature of 105°C. The permanently adhesive side still adherent the GaAs wafers front side serves as a protection. So we managed to prepare a flexible GaAs wafer with a residual thickness of 25 µm.

4) DbyT for thin GaAs wafers: As latest technological work the experiences in handling and thinning of silicon wafers were transferred and applied to GaAs (100) substrates. According to the "DbyT"-concept GaAs (100) wafers were temporarily mounted on rigid carrier substrates. Based on formerly published results front side grooves and via holes defining the chip area and thickness are etched in an immersion etching process after a lithographic step [3, 4,5]. We compared two etching solutions for their shape of the etched cavities and their etching rates (fig. 4a,b). The cleavage direction was the (110) plane and in this case ordinary mesa shaped profiles of the residual GaAs and calotte shaped cross-sections of the etched trenches are received. The H_2O_2 (30%) / H_3PO_4 (%) (1:1) (fig. 4a) system provides high quality etched GaAs surfaces with well defined profiles and flat etched bottoms unfortunately degrading typical device contact metallization [5]. The etch rate was 17 µm/min. The second etchant medium [3] containing HF (40%) / HNO_3 (65%) / CH_3COOH (100%) / H_2O (1:3:2,3:2,5) (fig. 4b) removes GaAs nearly 4 times faster at an etching rate of 63 µm/min at room temperature. The edges are rounded calotte shaped with a higher slope as compared to the phosphoric etchant, enabling an subsequent smoother via-hole and backside metallization process.

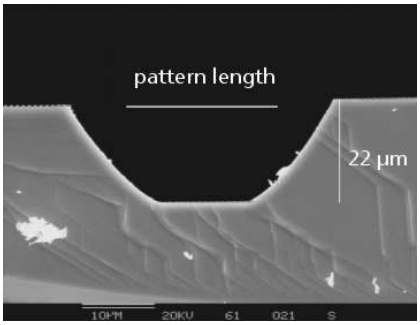

Figure 4a: etching profile of GaAs (100) etched in the H_3PO_4 - system

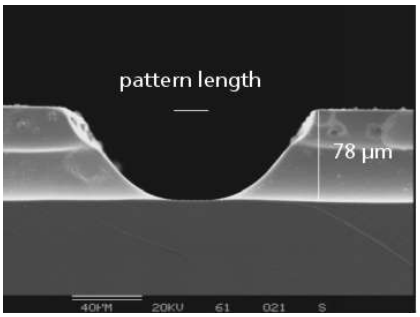

Figure 4b: etching profile of GaAs (100) etched in the HF - system

Subsequently the GaAs wafer was temporarily fixed on a perforated carrier substrate. In this case a resist serves as an adhesive. The backside spin etching process was prepared by the method described above. Chip separation occurs when finally the front side grooves are opened. In order to take the chips a solvent penetrates the perforated carrier and dissolves the adhesive. On this way chips with a thickness of 15 µm and differently sized via holes are prepared (fig. 5a-c).

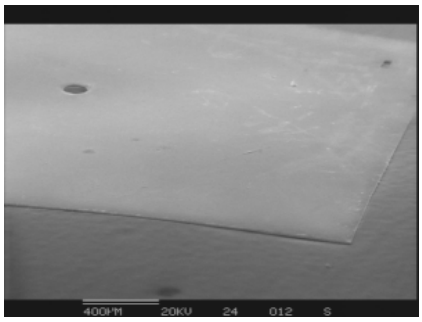

Figure 5a: ultra thin GaAs-chip with via hole prepared according to "DbyT"- concept (thickness: 15 µm)

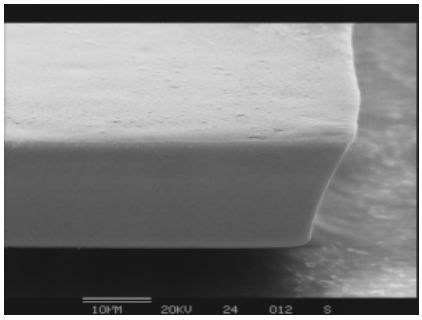

Figure 5b: ultra thin GaAs-chip edges (thickness 15 µm)

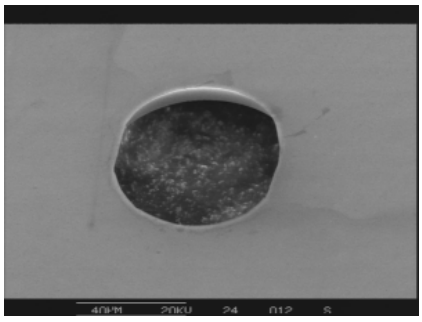

Figure 5c: ultra thin GaAs-chip with via hole of 50 µm prepared according to "DbyT" – concept (thickness: 15 µm)

NOVEL HANDLING CONCEPT FOR THIN WAFERS "SMART CARRIERS"

Handling and processing of fragile wafers in the thickness range below 100 µm is a challenging task for a production environment. To minimize the risk of breakage thin wafers are often temporarily fixed to a support substrate. Widely used in GaAs manufacturing are thermoplastic glues, e. g. wax, and ceramic carriers, which also might be perforated to enhance solubility of the glue layer during the final de-attach process. Strongest drawbacks of the known wax techniques are the need for subsequent cleaning steps and the limited temperature stability of organic adhesive layers. These disadvantages will be overcome by introducing an electrostatic holding principle that allows for free handling and processing of thinned device wafers: "Smart Carriers" [6, 7].

1) Principle of an electrostatic carrier: Electrostatic attractive forces are used since many years within electrostatic wafer chucks (ESC) inside of vacuum dry etching systems (see for example [8]). An electrostatic pattern (inter digital structure or opposed multi-pole areas) is covered by an insulating dielectric layer. By applying high voltage (1 .. 3 kV) to the ESC an electrostatic field is generated which attracts the semiconductor substrate towards the wafer chuck.

If the cover layer is a material of high polarizability the electrical fields remain active also after disconnecting the external power supply of the ESC. Thereby the electrostatically activated plate can be used as a mobile holder for a wafer. By choosing a wafer shaped geometry the "Smart Carrier" can be handled with standard robot and cassette systems.

"Smart Carriers" may be manufactured on the base of rigid polymer tapes, e. g. polyimide, or on ceramic substrates. Latter one offers the possibility for the electrostatic carrier to be used during high temperature processes.

First demonstrators of a "Smart Carrier" were realized using alumina plates with a screen printed thick film metallization pattern, covered by a dielectric layer. Figure 6 shows an example of a 6 inch carrier substrate holding a GaAs wafer of 3 inch diameter and 100 µm thickness. The electrostatic structure pattern of this demonstrator was designed as a intercepting finger pattern. The capacity of the carrier can be charged by a power supply at two connection pads, which are located either at the edge or at the backside of the ceramic plate.

Figure 6: First demonstrator of an electrostatic support substrate: "Smart Carrier", holding a 3" GaAs wafer.

2) Applications of “Smart Carriers” for handling and processing of thinned wafers: Material properties of semiconductor substrates of a thickness below 150 µm make the electrostatic principle ideally suited to be used as a reversible support technique. First, thin wafers are pliable, their flexibility guarantees for very narrow gaps between the contacting substrate surfaces. Thus the rapid decay of the electric field at larger distances from the electrostatic pattern shows minor influence. Secondly, thin wafers are of light weight and therefore don’t need high bonding forces. So thin device wafers can be hold securely even at a moderate strength of the electric fields. Or in other words the unavoidable time depending decrease of the electric capacity doesn’t prevent the bonding effect for a certain period of time. The related time constants are depending on the temperature and the material properties of the cover layer. With the first demonstrators thin wafers could be fixed to a “Smart Carrier” for several days at room temperature. Also spin-coating and hotplate baking up to 150°C was applicable for device wafers, which were supported by an electrostatic carrier. Figure 7 shows a wet-chemical spin-etching process of a 100 µm thin silicon wafer, fixed to a “Smart Carrier”.

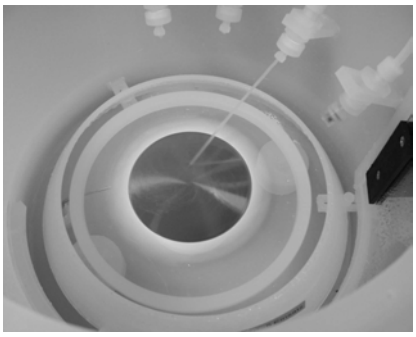

Figure 7: Application of electrostatic carrier substrates during wet-chemical spin-etching of thin wafers.

3) Technological aims for “Smart Carriers”: Further development work will concentrate on the improvement of the time and temperature stability of the polarization of the cover layer. Project target is the demonstration of secure handling and processing of thin wafers by means of “Smart Carrier” substrates at temperatures up to 400°C for 30 minutes. The Smart Carrier development will be performed in close cooperation with the company ProTec GmbH [9].

CONCLUSION

Appropriate manufacturing technologies play an important role for new microelectronic devices which are intended to be thinned down to a remaining thickness of 20 – 50 µm. Beside the wafer thinning itself dicing processes must ensure crystalline quality at the chip edges. The concept “Dicing-by-Thinning” allows preparation of ultra thin dies both for silicon and for gallium arsenide substrates. Especially in the case of small die sizes the “DbyT” concept together with dry etched chip separation grooves allows for a strongly increased amount of chip products per wafer.
The new technological concept “Smart Carrier” is supposed to become a cost effective solution for handling and processing of wafers in the thickness range below 100 µm. Its most valuable benefits are multiple use, elimination of polymer adhesives and the capability for easy attach and de-attach of carrier substrates. The electrostatic principal solely offers the perspective of a reversible support technique for ultra thin wafers which is also applicable to high temperature processes.

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