A Novel Backside Process to Achieve 1-mil Thick Wafers at 6-inch Foundry

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Abstract

A manufacturable 1-mil backside process with high quality and high yield has been successfully developed and demonstrated at WIN Semiconductors' 6-inch foundry to accommodate customer's need. The key differences between the existing 4mil/2mil backside process and the newly developed 1-mil process are compared and discussed. Modified mount/ demount and cleaning procedures to reduce the thermal shock are presented. It has been found that stress reduction of plated Au films with the plating condition optimization and the increase in Au thickness for supporting are effective in reducing the 1-mil wafer breakage rate. A selective plating process has also been implemented on the 1-mil wafer to ensure a higher backside yield. Greater than 95% scribe and break yield has been achieved with excellent quality after optimization on the scribe and break process.

INTRODUCTION

WIN Semiconductors provides dedicated HBT and pHEMT foundry service with advanced 6-inch MMIC process technologies. High quality, yield, and cost effective manufacturing with full customer satisfaction is the key for a successful foundry. To fulfill customer's requirement at many varieties of applications, WIN has committed constant process development and improvement to achieve state-of the-art technologies.

Market requirement for increased RF performance; higher power and improved thermal dissipation have necessitated optimization, not only in frontside, but also in the area of backside processing. Even though the reduction in wafer thickness will get a great improvement in heat dissipation for better device operation and performance, the ultra-thin wafer is a challenge in backside process. WIN's 6-inch HBT and HEMT technologies with 4-mil and 2-mil backside process have been routinely fabricated and delivered to customers with high visual and electrical yields. Recently, customers have a request for a 1-mil thick technology for their high power and high voltage applications. A task force was formed to develop such a technology to fulfill customers' need. In addition, the new technology needs to be compatible with our current 4-mil/2-mil backside process to ensure the manufacturability and reduce the cost. In this paper, we will discuss the approaches to develop such a process; the difficulties and challenges that we faced during the development, and the final released process and results.

CHALLENGES IN BACKSIDE PROCESS

Wafer crack and breakage are the major yield-killers in the backside thin-wafer process; therefore, the key factor to achieve ultra-thin wafer is to reduce the stress or shock to the wafer as much as possible. This is a complicated mechanism since the stress could be induced by the material added on the wafer or the process step itself. We might not see the effect at the step where the large stress introduced on the wafer, but its damage shows up at the later process stage and causes wafer breakage, which is hard to trace back. Therefore, we have to re-evaluate the entire backside process steps, and then implement necessary major and minor changes at various steps to successfully develop the new 1-mil backside process. Figure 1 and 2 showed the comparison of the major process flow for our current 4mil/2mil backside process and the newly developed 1-mil process. The key differences between the two processes will be discussed in this study.

MOUNT AND DEMOUNT PROCESS

The most severe thermal shocks on the wafer during the backside process happen at the mount and demount steps. Wax needs to be heated from the range of 100°C to 200°C to adhere the wafer with the sapphire. After completing the wafer thinning, backside Via, Au plating, and backside street formation, the thinned wafer need to be demounted from the sapphire. Thermal or high temperature solvent was used to melt or dissolve the wax to separate the wafer

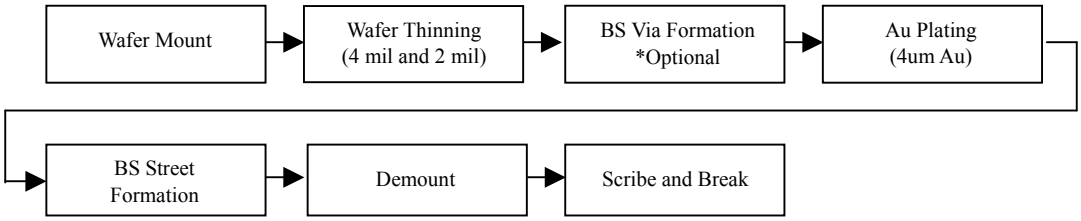

Figure 1 Standard 4-mil/2-mil 6-inch backside process

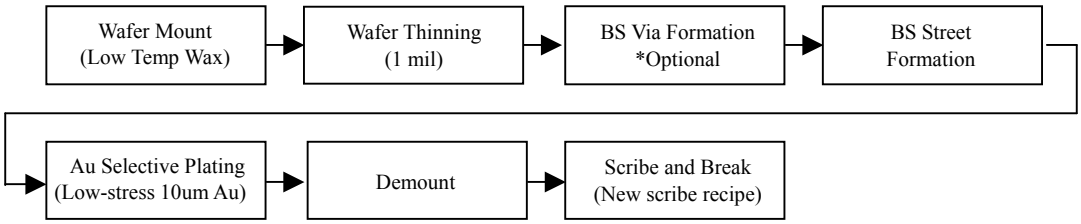

Figure 2 New 1-mil 6-inch backside process

from the sapphire.

The standard mount and demount procedures and process parameters on the 4-mil wafers were first tried on the 1-mil finished wafers. The yield dropped significantly with the wafer breakage to be the major yield loss. The wafers were still in one-piece right after the demount process, however, it often shattered during the cool-down or at the subsequent scribe and break steps. This suggests that the large stress could be built in the wafer during the thermal process steps; even though we might not see the impacts at the same step, but its damage shows up at the later process stage and causes wafer breakage. Therefore, to decrease the thermal shock during the mount and demount process will help to reduce the risks of wafer breakage.

A new wax with lower melting temperature was utilized in the 1-mil process to reduce the thermal shock during the wafer mounting and demount process. A modified cleaning procedure was also implemented to decrease the thermal shock. A spin-clean procedure with solvent spray was originally used in the 4-mil backside process. It was found that the solvent spray will absorb the heat from wafer surface and thus cause a quick temperature drop on the wafer to induce additional thermal shock. A modified solvent soaked clean was developed and used to eliminate this thermal shock and improve the 1-mil backside process yield.

AU PLATING

One of the key steps in backside processing is the electro-plating of a conformal gold layer on the backside surface and into through substrate Via holes. Backside metallization also provide the support to the ultra-thin and fragile 6-inch GaAs wafer. Reducing the stress from plated Au layer on the thinned GaAs and increasing the thickness of Au for supporting are the two factors to improve the 1-mil backside yield. In general, pulse plating was utilized to get a better Via hole step coverage, however, plating current spikes from pulse plating tends to create dendrites and degrades the plating solution lifetime[1]. Therefore, DC plating was used in this study to optimize the plating conditions and to investigate the thermal effects on the stress to achieve the lower gold film stress on GaAs.

The impact of plating current density on the Au film stress was first investigated. 10um thick Au was plated on a blank GaAs wafer pre-sputtered with the seed layer. The DC plating current was varied from 0.2 Amp to 1.5 Amp. The Au film stress was obtained with a Tencor FLX-2320 stress meter, which measures the curvature changes before (blank GaAs wafers) and after the seed layer deposition and Au plating. It is important to notice that the film stress need to be measured on the GaAs wafer with seed metal that is the same as the production wafer, since the film stress is very sensitive to the layer structures

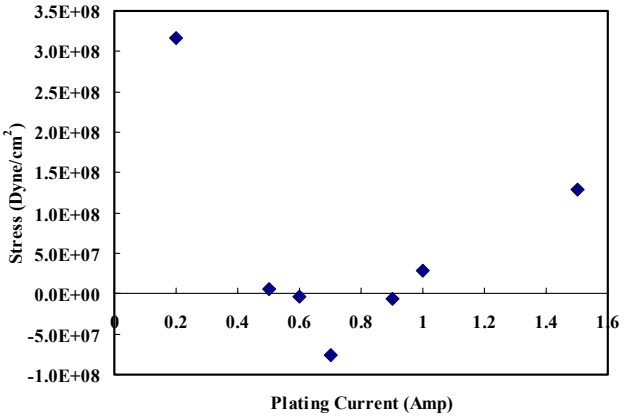

Figure 3 The effects of the plating current on the film stress

and the material that it grows on. Figure 3 shows the effect of the DC plating current on the film stress. It was found that the Au film stress increased significantly with both high and low plating current. Plating current between 0.6 to 0.9 Amp was the target current range in order to grow a low-stress plated Au film.

Our goal is to achieve the low-stress film on the final finished 1-mil thick wafer, therefore, it is important to study the thermal effect on the stress of gold film since the Au plated wafers will be subject to many temperature cycles during the subsequent process steps like cleaning and demount. Figure 4 shows the changes in the film stress with three different temperature treatments. The test wafers were treated at various temperature and then cool down to room temperature for the film stress measurement. We could conclude from the plot that the Au film stress increased when wafer receive a higher temperature process cycle. Therefore, an optimized plating current combined with low-temperature cleaning and demount processes (as mentioned in the previous section) is the key factor to achieve lowest Au stress film on the finished 1-mil thick wafer to achieve a higher backside yield.

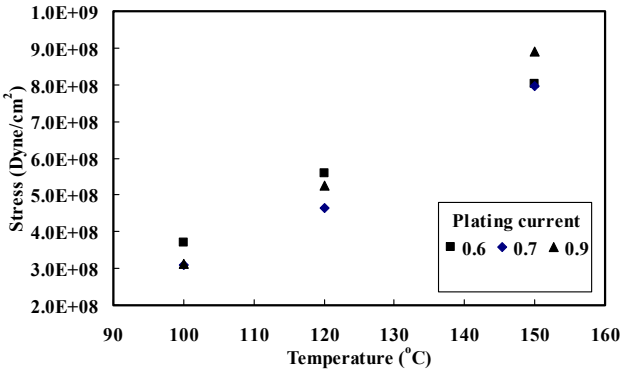

Figure 4 Plated Au film stress after thermal treatments

Backside plated Au also provides a support to the ultra-thin and fragile 6-inch GaAs wafer. Thicker Au layer could enhance the support and thus reduce the breakage rate. However, thicker Au would also increase the manufacturing cost. In addition to the cost issue, thicker Au layer induces a higher strain on the fragile GaAs material. To study the uniformity of the film structure and how the Au thickness impacts the average film stress, Au films with three different thicknesses were plated and the associated stress was measured. Table I shows that the film stress was essentially the same for the various film thickness, indicating a quite uniform plated Au film across the growth direction. Based on the results, 10um thick was chosen to be the target Au thickness to ensure a good support on the 1-mil thick wafer.

TABLE I
Plated Au film strain and stress with three different thicknesses.

Plated Au thickness (um)	4	7	10
Wafer bow (um)	6.8	16.6	49.6
Film stress (dynes/cm2)	1.29E08	1.57E08	1.47E08

To release the stress further, the selective plating process was utilized on the 1-mil wafers to replace the existing plating-and-etch process on the 4-mil and 2-mil wafers. The plating-and-etch is a simple process with fast cycle time; however, it first plates the wafer completely with Au films. This creates a higher strain on the wafer, which could induce internal stress. Even though the subsequent Au street-etch step will release the strain, the built-in damage resulted in a lower yield at the subsequent process steps. Therefore, a selective plating process was implemented on the 1-mil wafer to ensure a higher backside yield.

SCRIBE AND BREAK

Scribe and break is the most critical or yield-determinant step for 1-mil backside process since the wafers are close to the end of production. Not only it is the last process step but also the accumulated stress and damage could have a detrimental impact at this step since it involves lots of mechanical treatment. Scribe and break is a complex process that involves the optimization of numerous parameters [2] such as scribe force, diamond tool angle and speed, breaking force, breaking height and dwell time, and other machine dependent parameters. With so many variables, a design of experiments with Taguchi method has been carried out in our previous study [3] to find the optimal scribe force and scribe angle along the X and Y-axis on the standard 4-mil wafers. Scribe and break on the 1-mil thick wafer for sure needs more efforts and involve additional process optimization. A wafer with

higher internal stress accumulated from the previous process steps, would break or shatter when the diamond tool apply force on the wafers. Therefore, all the process consideration and optimization mentioned in the previous sections need to be implemented to ensure a successful scribe and break.

Various angle and forces of the scribe tool were studied on the 1-mil, 2-mil, and 4-mil wafers. It was found that the optimal angle on the 4-mil thick wafer could directly apply to the 2-mil or even 1-mil thick wafers. The optimal force, however, was very thickness dependent. Table II shows the optimal scribing force for the various wafer thicknesses.

TABLE II
Optimal scribing force for various wafer thicknesses.

Wafer thickness	4-mil	2-mil	1-mil
Optimized scribing force (gm)	30~40	25~30	15~20

Too much of the scribing force not only increase the breakage rate of the wafer, it also have a higher chance to "plow" the wafer (Fig.5a). A typical scribe methodology is to create a shallow "V" groove on the wafer surface along the crystal orientation, then the break mechanism actually separate the wafer. Too much of the scribing force will cut through the 1-mil thick wafer. This at first seems not an issue and it automatically completes the breaking step, however, the plowing line at one X-or Y-axis will cause the difficulty to the subsequent scribing in the other perpendicular axis. It generates chipping and debris to containment the chip surface and moreover damage the device area. The scribing quality on the first axis determines the scribing yield of the perpendicular axis and the subsequent yield.

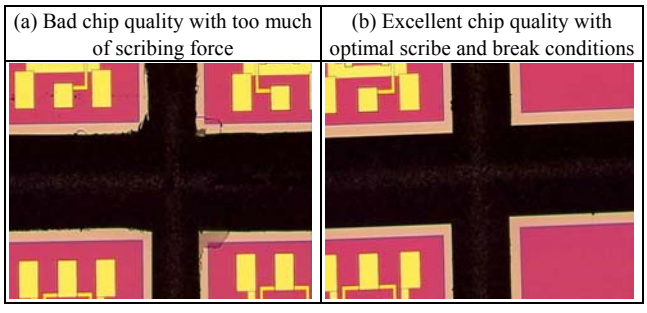

Figure 5 Chip appearances after scribe & break

After methodology and recipe optimization on the scribe and break step, a high yield was accomplished on the 1-mil thick wafer. Greater than 95% scribe and break yield has been achieved with excellent quality (Fig.5b).

CONCLUSIONS

In summary, to accommodate customer's need, a novel 1-mil backside process has been successfully developed in three months. A new wax with lower melting temperature together with modified cleaning procedures was used to reduce the thermal shock during the wafer mounting and demount steps. Selective gold plating process with plating condition optimization to adjust the film stress on GaAs was implemented on the 1-mil wafer to ensure a higher backside yield. Greater than 95% scribe and break yield has been achieved with excellent quality after methodology and recipe optimization on the scribe and break step. Figure 6 shows the resulting 1-mil thick 6-inch wafer that has been fabricated, separated and mounted on UV-tape.

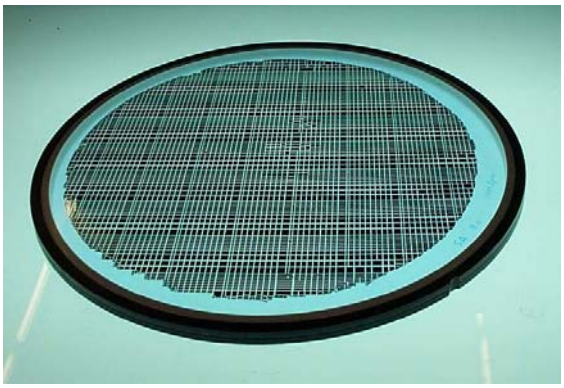

Figure 6 A completed 1-mil thick 6-inch wafer on UV-tape

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