Impact of Backside Via Dimension Changes on High Frequency GaAs MMIC Circuit Performance

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Abstract

This paper covers the impact of backside via dimension changes by utilizing ICP etching on the high frequency GaAs LNA circuit performance. New ICP tool offers improved repeatability and control of via size as compared to the existing RIE tool, but the via dimension significantly changed. Slight peak gain frequency shift to lower and gain slope change were observed by utilizing ICP etching, however, a narrow gain distribution was observed. Overall, ICP and RIE is not comparable process where the change of via dimension and consequent inductance change is sensitive to the circuit performance. Via dimension changes must be accounted for designs.

INTRODUCTION

The backside via is a critical element for MMIC technology. Electrically, it provides a low resistance contact to the common grounding plane and, at the same time, thermally serves as a heat dissipation path. Due to the nature of its through substrate etching, backside via etching is often a bottleneck of wafer production. Thus, an optimized process is strongly desired to improve the wafer throughput and to reduce the cycle time. Inductively Coupled Plasma (ICP) is a promising candidate for replacing conventional reactive ion etching (RIE) for GaAs backside via etching. Throughput improvement utilizing significantly faster etching rate was reported [1-2]. Furthermore, the ICP tools provide better control of via size and repeatability. A smaller size wafer e.g., 3 inch or less, the batch RIE tools may have an advantage in terms of throughput even with slower etching rate due to the multiple wafer processing capability. However, cost driven market keep demanding the larger size wafers and the ICP tools would be the choice for these larger size wafers.

The ICP tools produce significantly different via dimension as compared to the conventional RIE tools, if the same size mask used, due to its nature of etching process. Generally, ICP produces a vertical profile utilizing low pressure and higher ion density process while RIE produces a conical shape. Photo-resist (PR) sloping techniques, e.g., a high temperature baking, could introduce a tapered profile. However, even with the tapered profile, the completed via dimension may not be comparable with RIE. Recent studies utilizing different size of via dimension discussed the product performance improvement by shrinking the backside via dimension. Also, cost reduction was discussed by shrinking the die size through reducing the backside via dimension [3].

Minimizing source inductance is a critical issue for high frequency GaAs MMIC performance. Slight changes in source inductance could affect the circuit performance for higher frequency application. In particular, the low noise amplifier (LNA) circuits where source impedance feedback is often used as a means to achieve more stability may be more vulnerable to the subtle unwanted source inductance changes due to the change of via dimension.

For the implementation of new manufacturing technology like ICP backside via etching into the existing RIE etching production line, it is imperative to understand the impact of via dimension changes on the circuit performance. In this study, possible inductance changes due to different via dimensions and its impact on the circuit performance were studied.

EXPERIMENTAL

The higher frequency broadband LNA MMIC circuits utilizing monolithic 0.15 μm GaAs PHEMT, in a frequency range between 30 GHz to 110 GHz, were selected for a process split between RIE and ICP at the backside via etching step.

The GaAs PHEMT used in this study was grown on semi-insulating substrates by molecular beam epitaxy (MBE). The channel carriers are supplied by two-silicon delta doping. The 0.15 μm T-gate was fabricated by electron beam lithography and the gate recess profile was controlled by wet etch process. More detail overall process could be found at a previous publication [4].

The existing RIE system is a batch tool that could load up to six 3-inch wafers. The new ICP tool is a single wafer processing tool. Both RIE and ICP tool utilized Cl_2/BCl_3 gas chemistries. After a completion of the process, the circuits were characterized by s-parameter test

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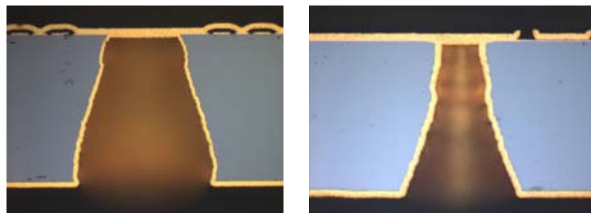
and noise parameter test to see the impact of inductance changes, if any, on the circuit performance.

RESULTS AND DISCUSSION

Via Dimension

Figure 1 illustrated comparison of the two via cross sections etched in RIE and ICP tools. The initial PR opening was 40 ± 2 µm. The shape of RIE via was conical and had some reentrance. The amount of reentrance varied slightly within a wafer and also a wafer to a wafer. The average via size was about 60 µm at the front side pad and 95 µm at the back. The shape of ICP via was tapered at the back of the wafer and rather vertical near the pad. The average via size was 37 µm at the pad and 75 µm at the back. The tapered profile was achieved by slopping PR, otherwise vertical without it, and is beneficial for subsequent metallization process. The ICP via hole has superior size repeatability over the RIE via hole. In particular, the foot size at the via pad was tightly controlled as a few micron less than the initial PR opening. This tight control of the foot size could provide more margin for shrinking the via pad size without risking yield loss due to a over-sized via.



(a) RIE via
55~70 µm at pad
85 ~105 µm at backside

(b) ICP via
37~40 µm at pad
70 ~80 at backside

Figure 1. Comparison of via dimension. (Thickness is about 100 µm)

RF Circuit Performance

Table 1 summarized the comparison of the gain of the tested circuits between ICP and RIE. As shown in Figure 2 to 5, a frequency shift (1 to 5 GHz) to lower, slight change of peak gain (0 to 1.5 dB) and gain slope changes were observed for the wafers etched at ICP. No noticeable change was observed for noise figure. The amount of s-parameter changes slightly varied circuit by circuit.

Table 1. Summary of gain comparison

Circuit	A	B	C	D
Circuit Type	Single Ended LNA	Balanced LNA	Single Ended LNA	Single Ended LNA
Ave. Peak Gain (dB)				
RIE	30.9	24.4	24.77	19.9
ICP	29.5	23.2	24.75	20.5
Peak Gain Freq. (GHz)				
RIE	41	57	54	105
ICP	36	56	50.5	102.2

Circuit A is a single ended LNA circuit. As shown in Figure 2, gain slope changed noticeably. For the RIE wafer, gain peaked at 41 GHz while gain peaked earlier at 36 GHz for the ICP wafer. Also, average peak gain dropped by 1.4 dB for the ICP wafer.

Both circuit B and circuit C was designed for use in about the same frequency range. Circuit B is a balanced circuit using Lange coupler to achieve more stability while circuit C is a single ended circuit. The layout of circuit B (2.7 mm x 2.1 mm) is significantly larger than that of circuit C (1.7mm x 0.9mm) by utilizing Lange coupler. Interestingly, Circuit B showed much comparable gain slope between ICP and RIE than that of Circuit C while the gain drops slightly more at higher end frequency for the ICP wafer (Figure 3). Circuit C showed not only a clear shift of gain slope but also its resonant type input and output matching (Figure 4). This different trend observed between the balanced circuit and the single ended circuit at comparable frequency range suggests that a specific circuit design methodology play a major role in mitigating the impact of inductance changes on circuit performance.

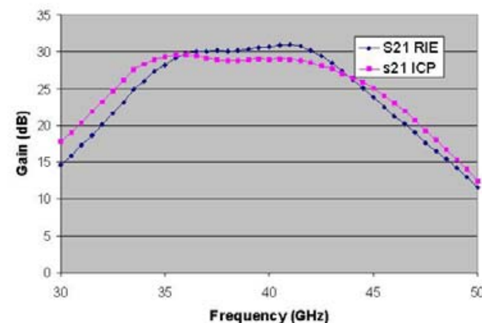


Figure 2. Comparison of measured gain for circuit A processed between ICP and RIE

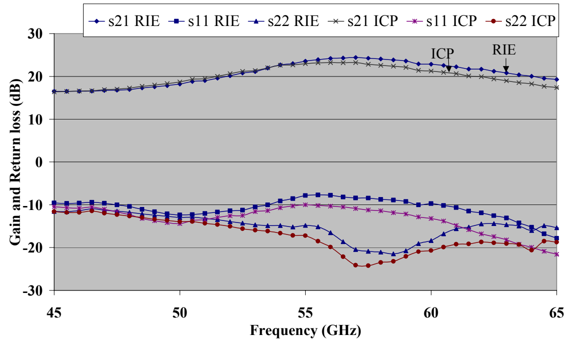


Figure 3. Comparison of measured gain and return loss for circuit B processed between ICP and RIE

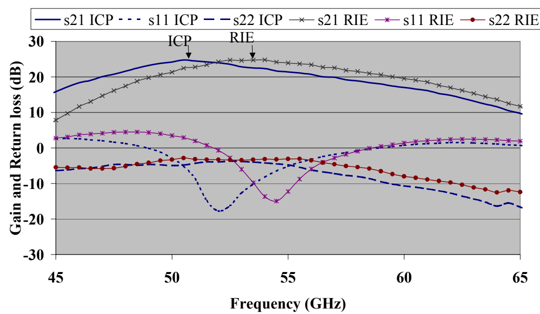


Figure 4. Comparison of measured gain and return loss for circuit C processed between ICP and RIE

Circuit D is a single ended LNA and has the highest frequency band among the tested circuits. Clear shift of gain slope was observed (Figure 5). About a 0.5 dB peak gain degradation was observed.

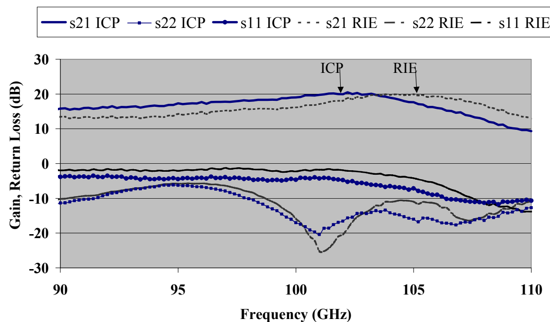


Figure 5. Comparison of measured gain and return loss for circuit D processed between ICP and RIE

Inductance

Unfortunately, there is no easy means to measure the backside via inductance directly. Electromagnetic simulation was often performed to evaluate the inductance. Via inductance generally increases when the via with higher aspect ratio is introduced. Previous backside via inductance study [5] reported a good match between the simulation value from the model and the extracted value from the test structure. It also predicted the increase of source inductance when via etching was switched from RIE to ICP due to the change of via dimension. The shift of resonant type of input and output return loss as shown in Figure 4 suggested the changes of impedance matching. Thus, the frequency shift of ICP may be attributed to the increase of source inductance and its influence on the impedance matching.

Gain Distribution

Figure 6 showed a histogram comparison for circuit A in peak gain distribution between ICP and RIE. Averaged peak gain dropped by 1.4 dB for ICP, but showed a narrow range of gain distribution. The standard deviation of peak gain was 0.87 dB for RIE and 0.57 dB for ICP. The other circuits also show superior standard deviation for ICP. Table 2 summarized the standard deviation. The enhanced homogeneity of the peak gain for ICP correlates with a better uniformity of via dimension in ICP as compared to RIE. Interestingly, Circuit B shows the smallest standard deviation among four circuits for both RIE and ICP and also shows the least discrepancy between RIE and ICP. Circuit B is designed as a balanced circuit and inherits less sensitivity to inductance variations. Thus, the inherent design methodology may mitigate the influence from the variation of RIE via dimension, resulted in comparable standard deviation with ICP as well as superior standard deviation as compared to the other circuits.

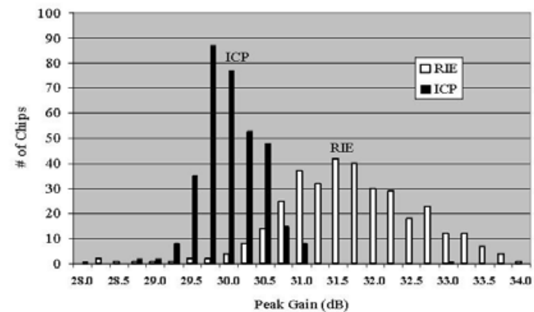


Figure 6. Histogram comparison of peak gain distribution for circuit A

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Table 2. Comparison of standard deviation of peak gain (dB)

STDEV	Circuit A	Circuit B	Circuit C	Circuit D
RIE	0.87	0.47	0.87	1.15
ICP	0.57	0.40	0.63	0.61

CONCLUSIONS

Implementing ICP via etching into the existing RIE production line may benefit from higher etching rate and better control of via dimension. However, the circuit data suggested that RIE and ICP might not be interchangeable processes with a straightforward manner for higher frequency applications where via inductance is more sensitive to the circuit performance. Via dimension changes must be accounted for designs. Also, process developments for comparable via dimension is required for the interchangeable process between RIE and ICP.

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ACRONYMS

ICP: Inductively Coupled Plasma
RIE: Reactive Ion Etching
MMIC: Monolithic Microwave Integrated Circuit
PHEMT: Pseudomorphic High Electron Mobility Transistor
LNA: Low Noise Amplifier

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