Dry Etching of Deep Backside Vias in InP

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Abstract

For the last several years, there has been great interest in InP HBTs due to the attractive properties of InP and its lattice matched materials used for high-speed digital circuit fabrication. Based on the successful introduction of high performance circuits on GaAs with backside vias, the same approach has been used for InP. The purpose of this work is to present results from dry etching of deep backside vias in InP in a high density, inductively coupled plasma reactor. All etching has been carried out on 3-inch wafers mounted on sapphire carriers. Our results show ~100µm deep vias with good profiles, average InP etch rates of 1.5µm/min and selectivities of InP to mask (photoresist) ≥10:1. This process is acceptable to introduce to our manufacturing environment.

INTRODUCTION

III-V backside processing is highly mechanical and in many cases non-automated, thus posing several barriers to high volume manufacturing. Significant advances have been made in the case of GaAs with a variety of processing equipment, mounting schemes and overall process control so that high yields are assured [1,2,3]. Borrowing from that knowledge base, the expectation is that InP backside processing can be very similar to that of GaAs. However, due to the high temperature plasma etch demands for InP (so that acceptable etch rates can be achieved), several barriers to manufacturability exist.

The backside process flow involves several steps: wafer mount and thinning, photolithography and plasma etch, resist and residue removal, metallization and dismount. In this work, we will mainly focus on the plasma etching part of the process. Significant effort has been spent on developing an appropriate mounting/dismounting scheme for InP which enables the deep via etch. This is a potential barrier to manufacturability and its importance cannot be overlooked.

The goal for backside via etching is to successfully etch through the substrate and stop on the frontside metal which is usually a Ti/Pt/Au stack. The vias have to have relatively smooth sidewalls and bottoms and should be slightly tapered so that subsequent Au plating can cover everything adequately so there are no voids or discontinuities. The InP substrates we have been working with are generally thinned down (from the wafer backside) to between 100-130µm after the frontside has been fully processed and coated with a protective film. The wafers are mounted on sapphire carriers frontside down and after thinning they go through photolithography where the backside via pattern is defined. Then they are ready for plasma etching. The equipment used for all our etching experiments is Trikon's Omega® 201 ICP high density system (Figure 1) with a hot ESC (Electro-static Chuck). In this paper, we will show that our plasma etch process enables backside vias in InP.

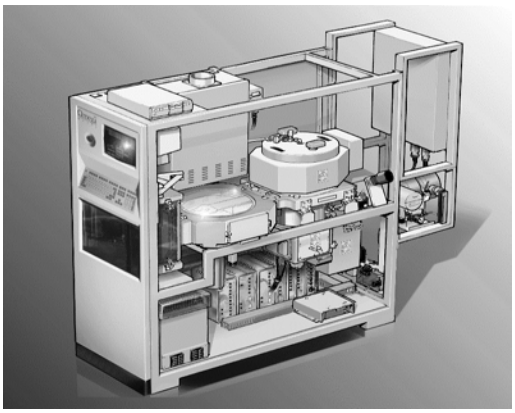

Figure 1. The Trikon etcher used for all InP dry etches.

RESULTS AND DISCUSSION

It is well known [4,5,6] that InP etches very slowly at ambient temperatures. In order to get average etch rates of 1.5µm/min for 100µm deep vias, we have found that the InP wafer temperature needs to be around 180°C. That is why we have chosen an ESC capable of operating at high temperatures (80-200°C). Our carrier/wafer is electrostatically clamped to the bottom rf electrode with enough He flowing between the backside of the carrier and the electrode for cooling.

In general, there are two approaches for etching backside vias in InP: (1) using a Cl_2–based chemistry or (2) using an HBr-based chemistry. They both work especially since $InCl_x$ and $InBr_y$ etch by-products tend to be more volatile as the temperature is increased [7]. Some of the criteria to be used when selecting an etch chemistry are: (a) what type of mask is being used; (b) what is the selectivity of InP to the mask; (c) how clean is the etch (what is the MWBC (Mean Wafers Between Cleans)); (d) how reproducible is the etch.

The type of mask used significantly affects the overall etch and the via profiles. From our experience, HBr-based chemistries have the advantage of being more photoresist-friendly than Cl_2-based chemistries. However, a disadvantage of using photoresist as a mask is the deposition of significant amounts of residue in the chamber, thus lowering MWBC. To address this issue we routinely use O_2 plasma cleans after each run to minimize chamber deposits. There is also a constant balance between deposition and etch that needs to be paid attention to in order to avoid etch stop or grass formation.

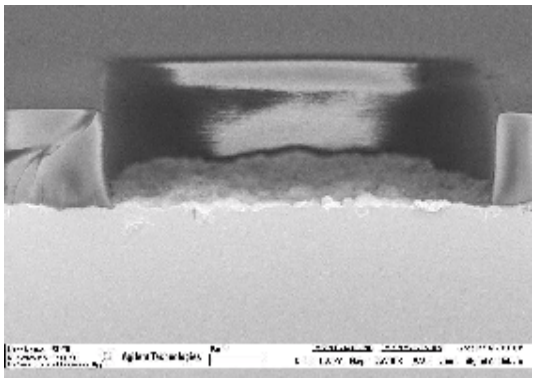

Figure 2. Micrograph of via feature (CD is 70 µm) with the thick photoresist mask before the dry etch.

Before etching begins, the via features using a photoresist mask are represented by the micrograph in Figure 2. For etching through ~100µm of InP, an average etch rate of ~1.5µm/min (or higher) should be targeted with a selectivity of InP to mask of ≥10:1. As seen in Figure 3, using an HBr-only chemistry, good profiles can be obtained with clean sidewalls. In this work, we have kept the inductive power constant and high and varied the rf-biasing power until an optimal condition was reached. Other variables such as total gas flow and pressure have also been investigated. One of the significant issues in this etch is ARDE [8,9] (Aspect Ratio Dependent Etch). Figure 4 is a good example of this showing vias of varying size on the same mask. The smallest vias etch the slowest. In Figure 5, the InP average etch rate is plotted versus via size and it is clear that there is a difference in the final via depth depending on size. For best results, backside via masks should be populated with vias of the same size.

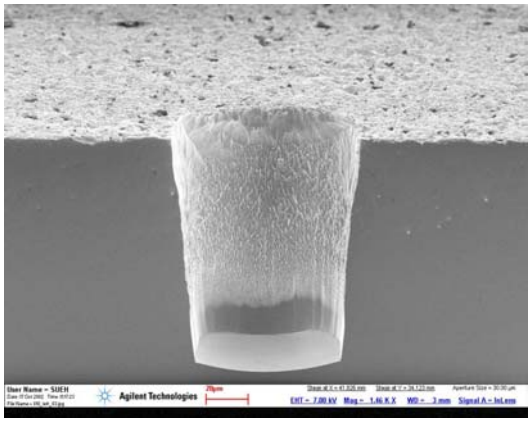

Figure 3. This is an example of a backside via in InP (etched in HBr-only). The photoresist mask has been removed. The sidewalls are fairly smooth with a square bottom profile. In this case, via depth is ~110µm and width at the bottom is ~80 µm.

The effects of rf bottom electrode power on wafer temperature have been well documented [8]. Even though we did not use more sophisticated means for temperature measurement than just appropriately placed and protected temperature dots, we produced trends very similar to those reported in the literature. Figure 6 illustrates this well. In this particular experiment, the ESC temperature was held

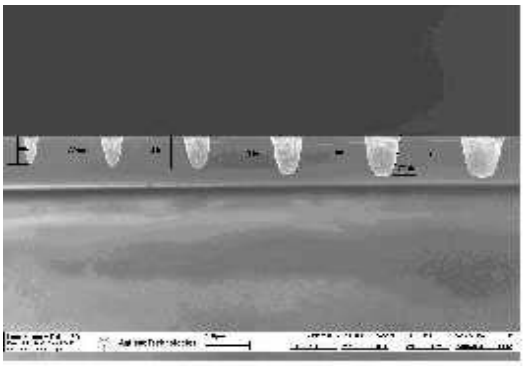

Figure 4. ARDE. This particular via chain goes from 30 to 80 µm in increments of 10µm in CD. This is an HBr-only etch and a photoresist mask was used which has been subsequently removed.

constant at 130°C and the rf-bottom electrode power was varied. As can be seen from the graph, the samples were left in the chamber for ten minutes to equilibrate at the ESC setpoint temperature. The plasma was not on during the equilibration time. After that, the plasma was turned on and data collected for a maximum of 10 additional minutes. This same graph shows that at the same rf bottom electrode power of 90 Watts, dropping the ESC temperature by 20°C does have the effect of lowering the overall wafer temperature. In all cases, as mentioned earlier, backside He is flowing for cooling. The overall trend is that as higher bottom electrode rf power is applied, the higher the wafer temperature achieved due to increased ion bombardment. Another result from the above experiment is that wafer temperature is also affected by the ESC setpoint temperature.

There is a delicate balance between bottom electrode rf power and ESC temperature. One can lower the ESC setpoint temperature and increase the rf power or vice versa. However,

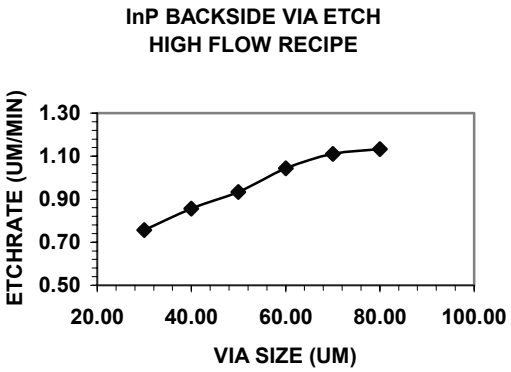

Figure 5. ARDE effects on etch rate.

when the wafer temperature gets too high, highly isotropic profiles can be obtained and the via profiles can be hard to control. Too low of rf bottom electrode power and etch stop or severe micromasking can occur. From our work, we have seen that 20 Watts difference in applied rf bottom electrode power between otherwise identical etch runs can cause an InP etch rate difference of 50-60%. There is an additional way to increase wafer temperature. He backside pressure can be minimized. The approach using this variable is to optimize He flow for the particular carrier/wafer stack one is working with, as well as for the particular ESC hardware in the reactor.

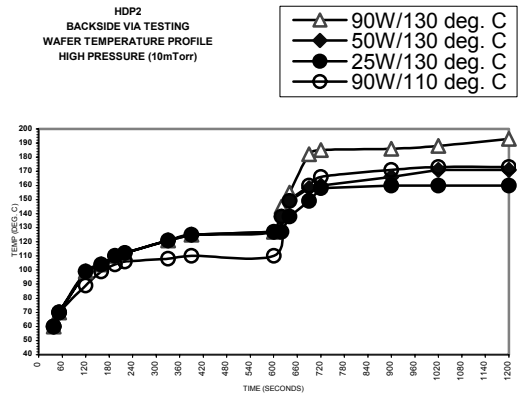

Figure 6. HBr-only chemistry with ICP power fixed at 900 Watts and chamber pressure at 10 mTorr.

We have found that we can consistently get an InP average etch rate over a total depth of approximately 100µm of about 1.5µm/min , with a selectivity of InP to the resist mask of about 10:1. Our experience thus far is that the resist etch rate when using an HBr chemistry is fairly consistent. However, one can loose InP etch rate very quickly and the deeper the vias the slower the etch rate becomes. A drawback of selecting slow InP etches is that in a highly polymerizing chemistry regime it is easy to get etch stop since there is significant deposition. This can be especially problematic when the etch is purposely stopped for via depth inspection (due to lack of good, automated endpoint capability). Due to the significant accumulation of etch deposits, when wafers are re-introduced to the chamber for additional etching, the semiconductor etch rate is dramatically reduced down to a fraction of a micron/min. Either a change in the recipe or a long, additional etch are needed in order to clear the vias all the way to

the frontside metal contact. Thus, the rule of thumb for a reasonable, manufacturable process is to keep relatively high semiconductor etch rates, ensure that the etch process itself has good uniformity across the substrate and have uniformly thinned wafers so that the semiconductor thickness is in good control. Another key to success is frequent O_2 plasma chamber cleans as mentioned earlier. For now all our etches are timed and since we need to stop on Au (part of the frontside metal stack) we do get some margin for the etch due to good selectivity of InP to Au (~8:1). Our best results (similar to Figure 3) are obtained with an HBr-only chemistry using a high ICP power and moderate rf bottom electrode power, high gas flow, moderate chamber pressure and an ESC setpoint temperature between 100-150°C. Although it is optional, the resist mask can be removed in situ and then the wafers can undergo an additional wet clean if necessary.

SUMMARY AND CONCLUSIONS

Using an HBr-only chemistry, we have been able to realize backside vias in InP. Our tool of choice for etching has been an inductively coupled plasma reactor (Trikon) with an ESC capable of high temperature operation. Good results have been obtained when the ESC temperature is set between 100-150°C. The average InP etch rate through ~100µm of depth is ~1.5µm/min and the selectivity of InP to the photoresist mask is consistently ≥10:1. These results make this process acceptable to introduce to our manufacturing environment.

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ACRONYMS

HBT: Hetero-junction Bipolar Transistor
ICP: Inductively Coupled Plasma
ESC: Electro-static Chuck
MWBC: Mean Wafers Between Cleans
ARDE: Aspect Ratio Dependent Etch

