Eliminating Pillars During GaAs Via Etch Formation

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Abstract

Pillar formation in GaAs vias is potentially harmful to reliable metallization. Pillar formation can arise from a number of causes including residues from upstream operations, material effects, and the plasma etching process. Using mechanical GaAs wafers, the plasma etch process contribution was partitioned through surface analysis and designed experiments. Pillar formation can be reduced through the use of higher Cl_2 flows, lower process pressures, and higher ICP powers. Lower RF bias powers during the etch initiation step also significantly reduced pillar formation.

INTRODUCTION

A commonly used process in the fabrication of GaAs devices is the formation of vias from the wafer backside to the frontside circuitry. Such vias provide a good thermal path for heat removal as well as a low ground impedance for RF (radio frequency) devices.

Ideally the backside etch process results in a via that has smooth sloped walls and clean surface at the frontside contact pad. In practice sparse grass formation (pillars) often occurs in a number vias [1,2]. These pillars are potentially harmful to reliable metallization of the via.

Pillar formation can arise from a number of causes including effects from upstream processes, material effects, and the plasma etch process itself. This article focuses on the effects of the plasma etch process on pillar formation. The formation of pillars during dry etching of GaAs through wafer vias was studied primarily using a BCl_3 / Cl_2 process in an inductively coupled plasma (ICP), though similar trends were observed in Ar / Cl_2 based processes.

Plasma etching of GaAs in a chlorine-based process follows an ion-assisted chemical etch mechanism. In a purely chemical etch process, the reaction etch products have sufficient volatility to spontaneously desorb from the surface. In an ion assisted process, desorption of the etch products can be assisted by ion bombardment (sputtering). Ion assisted chemical etch processes may involve the formation and removal of less volatile etch products as the etch proceeds. While Cl_2 plasmas will readily etch GaAs, a Cl_2 plasma alone often has trouble cleanly initiating the etch, prompting the addition of oxygen scavengers, such as BCl_3 or $SiCl_4$, to the process gas mixture. Ar / Cl_2 etch chemistries have also been used to successfully etch GaAs vias. A typical via etch process consists of two process steps: a physically driven etch initiation, and a chemically driven main etch. The etch initiation, a few microns deep in duration, typically contains a higher fraction of BCl_3 (or Ar) compared to the main etch and utilizes lower process pressures and higher RF bias powers. The goal of the initiation step is to cleanly start the etch, compensating for any surface damage or residuals from upstream processes (e.g. mounting & thinning operations). The main etch step typically runs at high Cl_2 fractions, higher gas flows, higher process pressures and reduced RF biases. The goal of the main etch is to quickly remove the material from the via while maintaining profile control and adequate selectivity to both the photoresist etch mask and gold etch stop.

EXPERIMENTAL

All wafers were etched in a Unaxis VLR 700 GaAs Via III Etcher. This cluster tool uses a 2MHz ICP source to generate a high density plasma. Ion energy at the wafer is controlled by independently biasing the cathode at 13.56 MHz. Wafer temperature is regulated by electrostatically clamping the wafer to a liquid cooled cathode in conjunction with He backside cooling. Plasma emission spectra were collected and analyzed using a Unaxis Spectraworks optical emission spectrometer (OES).

The substrates used in these experiments were 150 mm GaAs wafers patterned with a photoresist mask. The total exposed area of the test pattern was approximately 15% - a large portion of that area was due to a 2 mm photoresist edge bead removal required later in the process flow. The exposed via area was 7%. All depth measurements were performed using a step profilometer.

RESULTS & DISCUSSION

In order to partition upstream process effects from plasma etch induced effects, initial experiments were performed on mechanical GaAs substrates. In an effort to determine the causes of pillar formation, a sub-optimal (non-production worthy) process known to form pillars was used to generate via etch samples with high pillar densities. Previous work has shown that pillar formation can be correlated to substrate manufacturer [1]. During the course of this work a number of manufacturer's substrates were employed with appropriate controls to account for material effects.

A number of groups have suggested that pillars are caused primarily by residues present prior to etching or backsputtering of reactor components, particularly during the physical etch initiation, that act as "micromasks" causing pillar initiation. In order to determine if pillar initiation was due to micromasking a number of mechanical samples were partially etched (~ 10 µm depth) and subjected to SEM-EDX surface analysis. If reactor component backsputtering were responsible for pillar formation, newly formed pillars should have residual aluminum from either the aluminum chamber or ceramic (Al_2O_3) reactor components. While aluminum forms volatile etch products in a chorine-based chemistry, alumina (Al_2O_3) etching requires highly energetic ion bombardment and would likely remain as the etch proceeds. ***Figure 1*** compares the EDX spectrum from a newly formed pillar (***Figure 1B***) and cleanly etched GaAs feature (***Figure 1A***). Both spectra show the presence of Ga, As, Cl, and Au (samples were sputter coated with a thin Au/Pd layer prior to analysis to reduce charging effects). Notably absent in both samples were any peaks associated with aluminum.

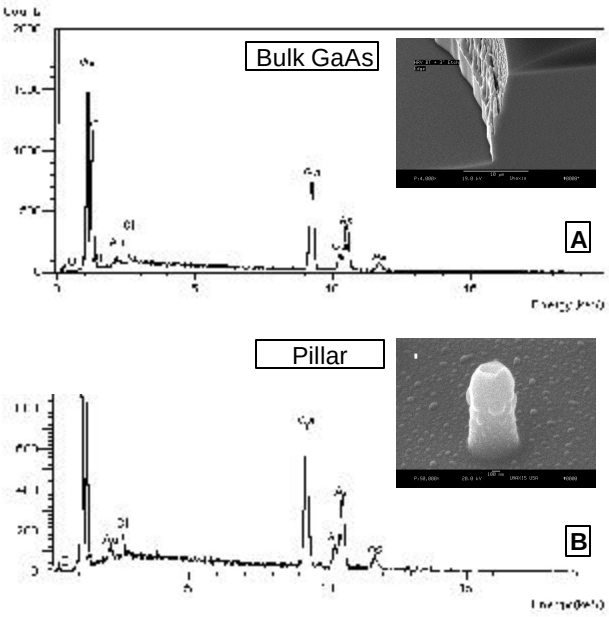

Figure 1 EDX spectrum from a newly formed pillar (**B**) and cleanly etched GaAs feature (**A**).

In order to determine when pillars are formed in the via etch process, a number of mechanical GaAs wafers were etched to different depths using identical processes and evaluated for pillar formation using SEM microscopy. The series of photos in ***Figure 2*** shows the etched GaAs surface at various time intervals. Based on the photos, pillars form near the transition between the etch initiation and main etch steps. The first two micrographs (***Fig 2A*** & ***2B***) show clean, defect free surfaces at the completion of the physical breakthrough process step and after one minute of the main etch respectively. The absence of pillars during the first few minutes of etching eliminates pre-etch surface residues as a candidate for pillar initiating micromasking. The third micrograph (***Fig 2C***) shows that small pillar defects of uniform height have formed after 2.5 minutes of the main etch step. The etch depth at this point in the process is 15µm and the pillars are 7 µm in height (pillar tip is 8 µm below the surface). In the last micrograph in the series (***Fig 2D***) the etch depth is 38 µm and the pillars are 28 µm in height (pillar tips are 10 µm below the surface). Given that some tip erosion has occurred as the etch proceeds it is likely that the pillars formed at the same time in both wafers. It is also important to note that since the pillar height distribution is monodisperse, all pillars on a wafer are formed at the same time. This provides further evidence against backsputtering of reactor components as the cause for pillar formation. The backsputtering of reactor components would be expected to continue throughout the entire process resulting in a continuous distribution of pillar heights.

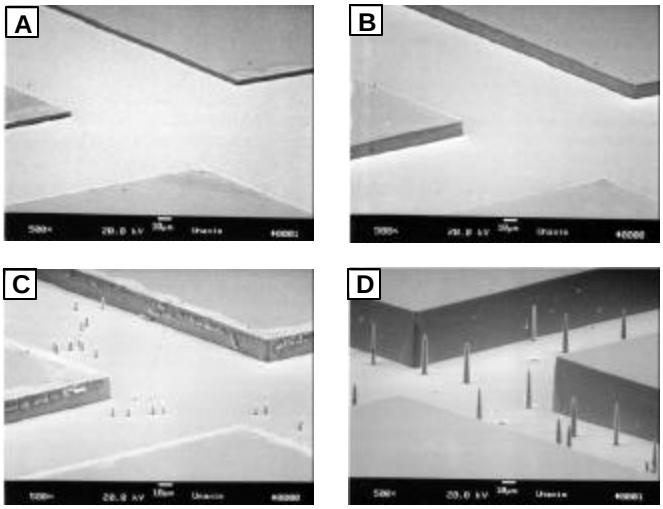

Figure 2 Etched GaAs surface at various time intervals: (A) after physical breakthrough, (B) after 1 min. of main etch, (C) after 2.5 min., (D) at an etch depth of 38 µm.

Once micromasking had been discounted as the primary cause of pillar formation for the test via etch process using mechanical wafers, a number of screening experiments examining process variables were performed. Total reactant flow (and consequently process gas residence time) was found to have a dramatic effect on pillar formation. ***Figure 3*** shows top-down optical micrographs of two features etched using identical chemistries, process pressures and RF powers but at different total gas flows. The features in the low flow (35

sccm – ***Figure 3A***) case showed significant pillar formation while the higher flow (350 sccm – ***Figure 3B***) case resulted in pillar free features. Both processes resulted in vertical feature profiles. As expected the high flow process resulted in significantly higher GaAs etch rates. ***Figure 4*** shows the relationship between GaAs etch rate and Cl_2 flow over a range of pressures and RF powers. To further investigate the differences between the high and low flow processes the plasma emission spectra of both processes were analyzed using optical emission spectrometry. ***Figure 5*** shows that the emission spectrum from the high flow process exhibits spectral lines for both the etch products (Ga, GaCl, etc.) and reactants (Cl and BCl). The emission lines from the reactants (the group of Cl lines around 750 nm) are greatly reduced in the spectrum from the low flow process.

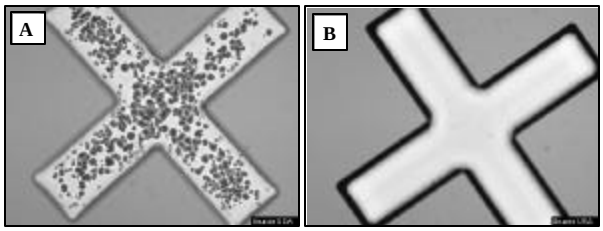

Figure 3 Top-down optical micrographs of features etched using 35 sccm gas flow (A) and 350 sccm (B).

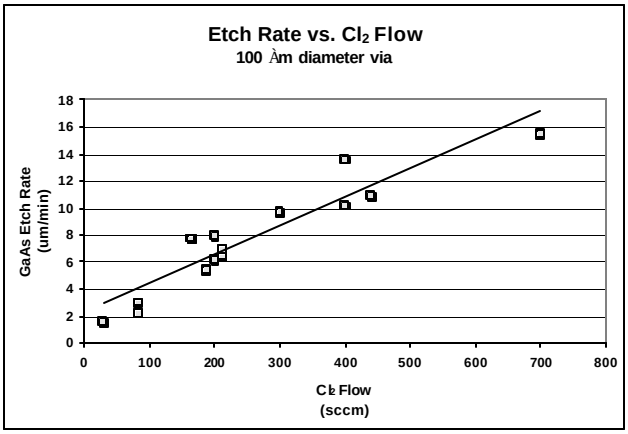

Figure 4 Relationship between GaAs etch rate and Cl_2 flow over a range of pressures and RF powers.

The effect of the etch process parameters on pillar formation was also investigated through a series of designed experiments. These experiments suggest that pillar formation can be reduced through the use of higher Cl_2 flows, higher ICP powers, lower process pressures, and reduced wafer temperatures. Based on these results, one possible mechanism for pillar formation during GaAs etching is through the creation of sub-chloride etch products. ***Table 1*** shows the relative volatility of potential GaAs etch products in a chlorine-based process. The formation of lower volatility sub-chlorides (i.e. $GaCl_2$ – b.p. 535°C) may momentarily act as an etch mask during the process, initiating pillar formation. While the precise reaction mechanism for GaAs in a Cl_2 plasma is not known, sub-chloride formation should be favored in a chlorine-deficient process regime. This theory correlates well with the emission spectra at lower Cl_2 flows (absence of Cl emission lines) and the designed experiments – high Cl_2 flows at lower pressures reduce the residence time increasing the concentration of reactants at the wafer surface. Increased ICP power should also increase the concentration of reactant at the wafer surface through higher dissociation of Cl_2. The observation of pillar densities increasing with increasing temperature however, does not appear to support the formation of sub-chlorides – higher temperatures should favor the desorption of lower volatility etch byproducts contrary to the observed relationship.

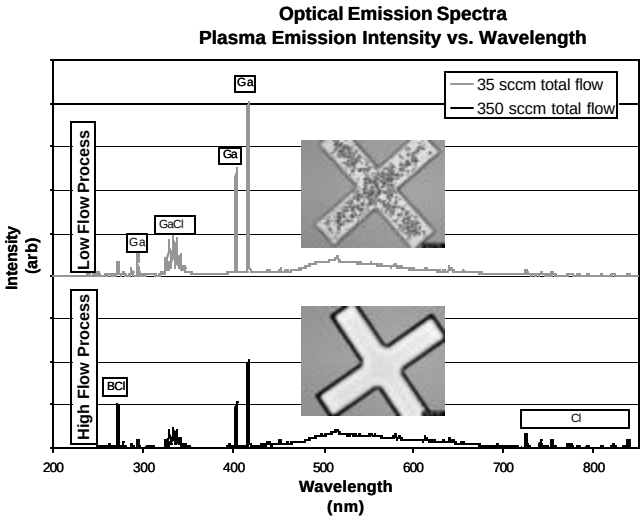

Figure 5 Emission spectrum from the high flow and low flow processes.

Component	Etch Product	Normal Boiling Point (°C)
Ga	$GaCl_2$ $GaCl_3$	535 201
As	$AsCl_3$	130

Table 1 Relative volatility of potential GaAs etch products in a chlorine-based process.

The designed experiments also showed that the RF bias power in the *etch initiation* step had a significant effect on pillar formation. This is consistent with the observation that pillars form immediately after the initiation step is completed (***Figs 2B & 2C***). ***Figure 6*** shows the pillar response versus the etch initiation RF bias power. Applying the results of the designed experiments to a high rate production via etch process resulted in an optimized etch process that produces pillar-free vias at GaAs etch rates of 10 µm/min (see ***Figure 7***).

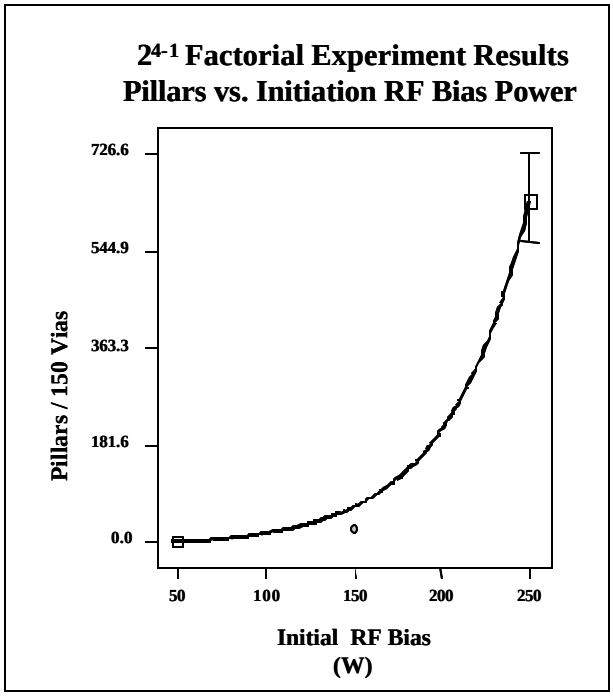

Figure 6 Pillar response versus the etch initiation RF bias power.

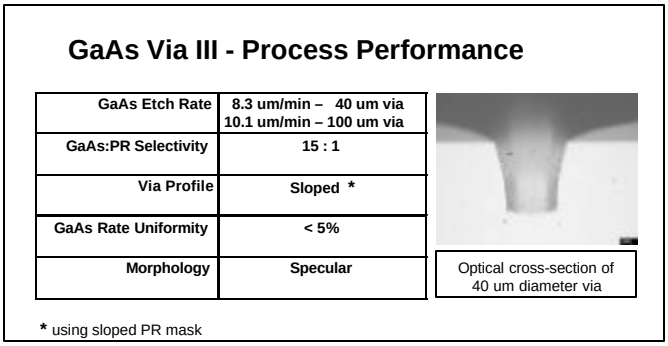

Figure 7 Optimized etch process that produces pillar-free vias at GaAs etch rates of 10 µm/min).

CONCLUSIONS

Pillar formation during GaAs via etching can arise from a number of causes including residues from upstream operations (grinding, mounting, photolithography, etc.), material effects, and the plasma etch process itself. Designed experiments have shown that pillar formation during the plasma etch process can be reduced through the use of higher Cl_2 flows, lower process pressures, and higher ICP powers during the main etch step. These results suggest that pillar formation may be due to the formation of lower volatility sub-chloride etch products ($GaCl_2$). This theory is reinforced by surface analysis that shows only Ga, As and Cl present at the tip of newly formed pillars. The observation that pillar formation is favored by higher wafer temperatures along with the fact that pillars are only formed at one point in the process do not lend support to this theory, consequently future work is required to reconcile these observations.

ACKNOWLEDGEMENTS

We wish to thank Mike DeVre, Yao-Sheng Lee, and Scott Klingbeil for their technical and manufacturing support of this work.

[1] Clayton F, Westerman R, Johnson D, *2002 GaAs MANTECH Technical Digest*, pp. 121–124.

[2] Nam PS, Ferreira LM, Lee TY, Tu KN, J. Vac. Sci. Technol. B **18**(6), pp. 2780-2784 (2000).

ACRONYMS

GaAs	Gallium Arsenide
RF	Radio Frequency
ICP	Inductively Coupled Plasma
Ar	Argon
Cl_2	Chlorine
BCl_3	Boron Trichloride
Ga	Gallium
As	Arsenic
OES	Optical Emission Spectroscopy
Al_2O_3	Aluminum Oxide
Au	Gold
Pd	Palladium

