In-Line Defectivity Methodology for a GaAs Manufacturing Facility

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ABSTRACT

Yield management based on in-line defect inspections must be implemented in order to be successful in a modern semiconductor manufacturing facility. This includes collecting large amounts of data that must be analyzed and maintained. Most fabrication facilities employ some form of defect inspection. Although often thought of as "non value" added inspections, a sampling plan must be realistic, provide meaningful data, and a mechanism for yield improvement. It is important to implement advance methods in defectivity and yield correlation to identify and address defects that result in yield excursions. This paper presents the implementation of a methodology that has resulted in increased yields and the reduction of yield excursions.

INTRODUCTION

Yield excursions can be complex with many different assigned and non-assigned causes. Until recently, defect-monitoring equipment at this factory was limited and data not full analyzed. This factory has installed two dark-field pattern recognition systems, a defect review station, and defect analysis computer. These tools allow the detection of defects on non-patterned films as well as patterned wafers. In addition, this factory also uses a high-resolution final optical inspection system to catch and classify defects from backend processing. With these systems this factory has been able to demonstrate the capability of defect review, classification, correlation, and its impact on yield.

This paper will focus on three main components of defect reduction and yield enhancement: defect excursion and control, yield prediction and module improvement. By collecting data in key locations within the process flow and feeding this information back to the process engineering groups, defects were reduced and new control limits on process equipment were set. This data collection program enabled a continuous reduction of defects in every group.

IN-LINE DEFECT SAMPLING AND YIELD MANAGEMENT

In-line defect monitoring is the process of measuring defects on wafers at predetermined stages as they are processed to detect and eliminate excursions that result in yield loss. Since it is not feasible to monitor 100% of all the wafers, a sampling plan is necessary. This factory chose to sample between 15-20% of the production line. The purpose of this sampling plan is to accomplish the following objectives:

1. Defect Excursion and Control

The purpose of this stage is to monitor on product defects at predetermined stopping points or modules to catch any defect excursions.

2. Yield Prediction

The objective here is to predict yields based on models developed and provide a feedback mechanism to process engineers.

3. Module Improvements

The purpose here is to learn about the different defects, classify them, and make process improvements to increase yield.

PARTITIONING THE LINE: DETERMINE WHAT LAYERS TO MONITOR

The defect inspection strategy was to first partition the line. Partitioning is depicted in figure 1: Partitioning the Line

Step	Description	Step	Description	Step	Description	Step	Inspection
★1	Inspection	★18	Inspection	35	Inspection	★52	Inspection
2	Surface Prep	19	Implant Photo	36	Via Photo	53	Metalization
3	Gate Metal	20	Implant	37	Via Etch	54	Inter Photo
4	Gate Photo	21	Deposition	38	Inspection	55	Inter Plate
5	Gate Etch	22	Inspection	39	Metalization	56	Inspection
★6	Inspection	23	Anneal	40	Metal 1 Photo	57	Pass Dep
7	Deposition	24	S/D Contact Photo	41	Plate	58	Pass Photo
8	Implant Photo	25	S/D Etch	★42	Inspection	59	Pass Etch
9	Implant 1	26	Inspection	43	Metalization	★60	Inspection
10	Implant 2	27	Deposition	44	Deposition		
11	Implant 3	28	Inspection	45	Cap Photo		
12	Inspection	★29	Liftoff	46	Metalization		
13	Deposition	30	Inspection	47	Liftoff		
14	Deposition	31	Probe	48	Inspection		
15	Inspection	32	Inspection	49	Deposition		
16	Etch	33	Deposition	50	Via 1 Photo		
17	Anneal	34	Deposition	51	Via 1 etch		

Figure 1: Partitioning the Line

Logical stopping points are inserted within the process flow within modules. Wafers are then scanned using dark-field pattern recognition system. Defect files are created and automatically transferred to a defect analysis computer where defects can then be reviewed and classified. Examples

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of process modules include gate formation, source-drain contacts and interconnect layers.

TOGGLING WAFER LOT STARTS

Lots that are to be monitored are automatically toggled at the wafer start stage. Since this factory is a paperless facility, electronically generated inspections steps are inserted in the process flow. During the track-out procedure of each identified inspection step, lots are automatically held for the yield enhancement team. All wafers are then scanned using a dark-field pattern recognition system. Three wafers are reviewed, and defects are classified. The defect densities are charted and plotted using SPC. If any control points are violated, see Figure 2: SPC Control Chart, then rapid response is taken. This could involve shutting a tool down or inspecting additional lots to verify the excursion.

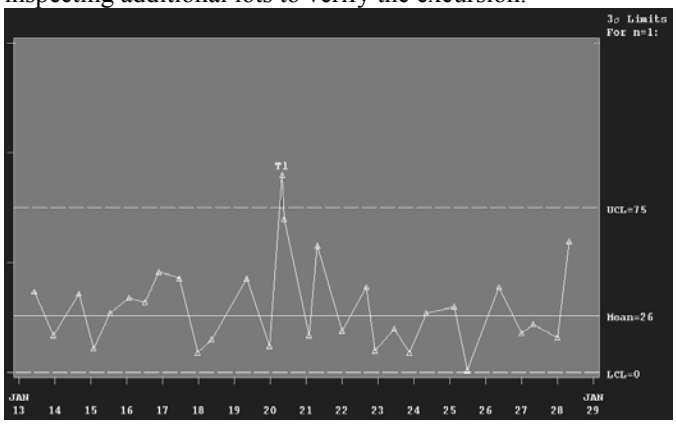

Figure 2: SPC Control Chart

THE DOW

Another system that is used to control defectivity, is to review the particle data with the process groups on a weekly basis. The data is monitored using the DOW, which is a composite of defects added per area and plotted for the factory. Setting continuous goals for the factory enables defects to be addressed, action plans determined, thus reducing the DOW. Each process group sends a representative or "defect champion" to these meetings. This representative is empowered to report back to his group with action items that are addressed and reported at the subsequent meetings. This is important to ensure, not only that defects are monitored, but also, defects are reduced on a continuous basis. An example of a DOW can be seen in Figure 3: The DOW.

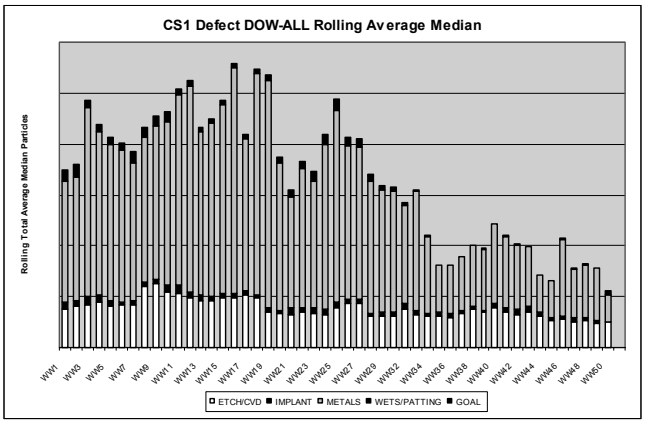

Figure 3: The DOW

DEFECT ANALYSIS

Collecting defect data and reducing defects does not always equate to improved yield. Analyzing all components of a defect is important in understanding the impact defects have on yield. Based on the analysis of the defect and the yield correlation, defect reduction projects can be prioritized. The use of in-line inspection tool that can measure defect densities and analyze the data to quantify the effect of the individual defect mechanism is an important ingredient in yield improvement. This can be accomplished by establishing a 'kill ratio" or probability yield. This includes identifying which die with a specified defect will fail electrical tests. These defects can be assigned "killer" or "non-killer" defect categories. It is important to determine which defects are "killer" from those that are "non-killer" or "cosmetic" such as color variation or metal grain variances.

There are three main components that are involved in this procedure: measurement, review and classification. The measurement of in-line product is performed on a dark-field micro inspection system and a map of the defects is generated. This map is transferred to a defect review station where the defects can be analyzed, classified, and cataloged for future reference. In any methodology it is important that defect libraries are created, defect classification is automated and catalog cards continuously updated. At this factory a defect library is used for easy reference and rejection criteria. In figure 4 a defect card catalog is given as an example of a defect map and the defects generated.

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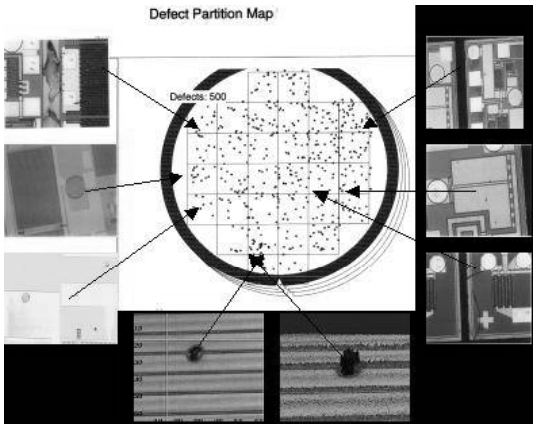

Figure 4: Defect Catalog

Defects can further analyzed using SEM and 3D laser imaging. Both of these techniques can be non-destructive. This factory utilizes both a SEM and a Confocal Review station, which uses both bright-field/dark-field white light microscopes with a laser confocal microscope and an imaging process computer. This gives the operator the ability to measure pits and particle depths against heights. Defects can be detected at the layer they occurred by the return of light intensity, which is a function of the material. On the live laser image the color of conducting material such as metal is usually golden in color while dielectric materials, such as oxide and photoresist are usually black or dark blue. An example of a carbon defect in Au deposited film is depicted in Figure 5: Laser Imaging and Cross-Section graph.

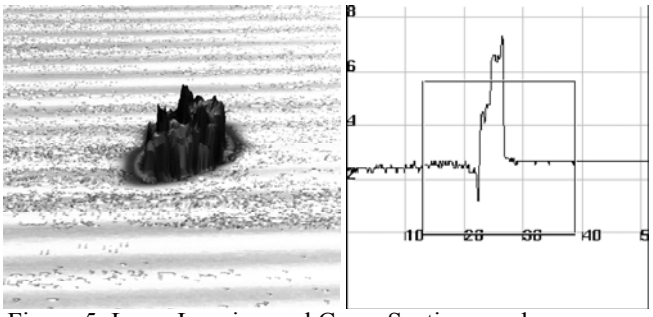
Figure 5: Laser Imaging and Cross-Section graph.

YIELD ANALYSIS

The purpose of yield analysis is to identify the areas that need additional controls to maintain high yields[3]. Yield analysis is an important tool in identifying the effect of defects and the resulting yield loss. However, because of cycle times the feedback is often long and may result in large amounts of scrap. Using in-line defect monitoring on product can provide extremely fast feedback to process engineers to correct the source of these yield excursions.

IN-LINE MAPPING CORRELATION

Since defect inspections are performed at various levels, defect equipment will often scan the same defect, especially if the defect is in a transparent layer. These defects can often become decorated and noticeable at later stages in the process. To address this issue defect analysis tools are used that can distinguish between added defects and previous defects. Each layer can be overlayed with previous layers so that one map represents the in-line defectivity failures. This allows for better yield correlation to defect densities. The stacked in-line map is then compared with the electrical map, see figure 6: In-line Mapping.

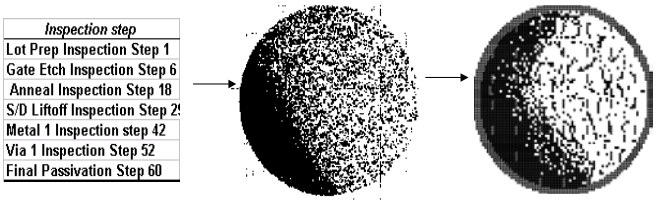

Figure 6: In-line Mapping

ACTIVE AREA ANALYSIS

Active area analysis provides the additional benefit of correlating defect densities with specific bin failures. Yield loss as correlated to defect density is presented in figure 7: Yield Loss Correlated to Defect Density.

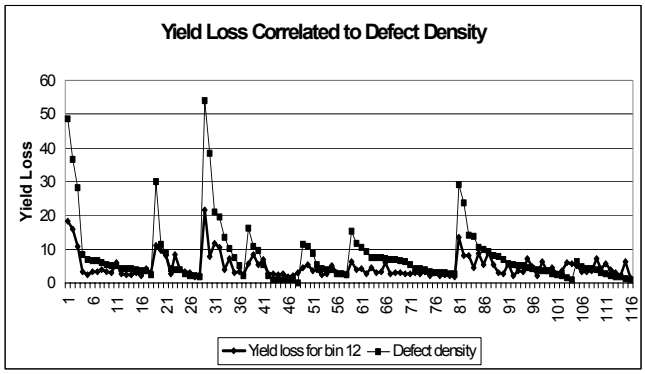

Figure 7: Yield Loss Correlated to Defect Density.

In addition, this factory uses active area analysis to predict the "killing probability" for different layers. Active area, wafer diameter and die size, are important inputs in establishing these yield models.

Many of the existing yield models are quite complex and many authors suggest that in-line data is too noisy to use in yield prediction [1,4]. Active area analysis is a quick and simple test that takes the die size into consideration. Using the active area from the photo mask and multiplying by the defect densities obtained from the process, it is possible to predict yield. This can be applied at every process level. The limiting yield for a process layer is based on the range of

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defects found using Poisson statistics from the following equation [5]:

$$Y_L = e^{-\sum AA_{II} \cdot DD}$$

where, AA is the active area and DD is the defect density.

Using these correlations probability yield can be compared to actual yield. Figure 7 demonstrates the use of such yield modeling.

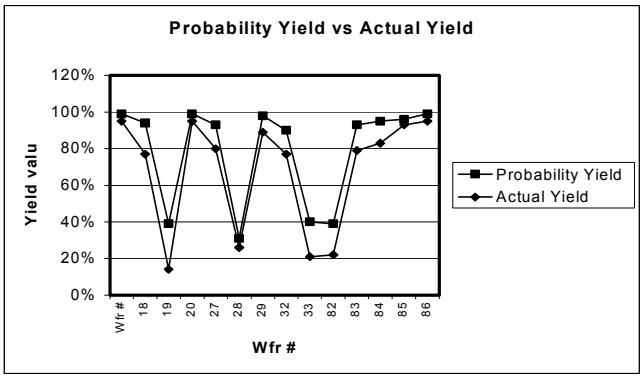

Figure 8: Probability Yield vs. Actual Yield

Plotting the probability yield and the actual yield can be quite useful in planning customer commitments and wafer start adjustments, as well as identifying future defect density reduction opportunities.

Finally, having the ability to compare unit probe, FOI, and in-line defects for a correlation of electrical data with optical inspection has resulted in an opportunity to address "killer" defects. The use of this methodology has enabled this factory to successfully address random yield excursions and reduce overall defects, thus increasing the cumulative yield.

ONGOING MEASUREMENT TECHNIQUES AND CHALLENGES

Variations in the process such as the roughness and inconsistency in some metallic films necessitates the need of alternative methods on yield detection. Modules within a process can create additional issues. A good example of this is a planar capacitor module that requires very low defect densities to obtain acceptable yields.

It is often necessary that short flows are developed to evaluate the "kill rate" of defects. These short-flow monitors, using less expensive silicon, are critical in the development and monitoring of sensitive modules such as the planar capacitor. These monitors provide immediate feedback to process and equipment owners. In many cases these monitors are added to production lots at the beginning of the process module.

SUMMARY

GaAs Fabrication facilities can implement inspection methodologies using limited resources. This paper suggested a methodology for sampling using partitioning and in-line defectivity analysis to determine "killer" and "non-killer" defects. Additionally, by using this methodology to compare predicted yield (using critical area analysis) with actual yield, defect reduction strategies can be implemented. Consistent monitoring of defects and reporting on those defects at weekly meetings is crucial in involving all areas and providing feedback on yield loss.

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ACRONYMS

FOI: Final Optical Inspection
SPC: Statistical Process Control
DOW: Defect on Wafer
SEM: Scanning Electron Microscope

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