High uniformity, highly reproducible non-selective wet gate recess etch process for InP HEMTs

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Keywords: WET ETCH, INP, HEMT

Abstract

A new non-selective wet etching technique has been developed to etch $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ structure for the gate recess of InP HEMTs. Both precise etch depth and well-controlled undercut width were achieved. Very smooth etched surface was also demonstrated by this new etching technique. 120nm gate length InP HEMTs were fabricated using this new gate recess process. A maxium transconductance, g_m of 660 mS/mm and current cut-off frequency, f_T of 250 GHz were achieved. Those devices performances are comparable to the best results we have achieved by using other gate recess technique. Finally, this new recess etching process is highly uniform and reproducible.

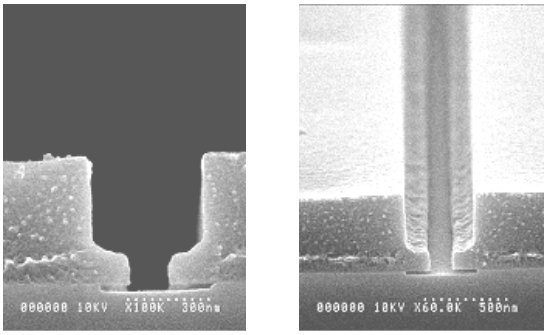
INTRODUCTION

InP based InGaAs/InAlAs HEMTs are considered to be one of the most promising devices for next generation millimetre wave and optical communications because of their superior high frequency and low noise performance. For the InP HEMTs, gate recess etching is the most crucial process because the gate recess structure fundamentally determines both performance and uniformity of the devices. The most widely used gate recess process is selective etching and many studies of selective dry or wet etching for InGaAs over InAlAs have been reported.[1] However, by using selective recess etching, the distance between gate and channel, which is crucial to device performance[2], is solely dependent on the thickness of the InAlAs layer. This greatly decreases the flexibility of device design and process control. Furthermore, selective gate recess etching processes for InP HEMTs suffer additional problems. For selective dry etching, although excellent etch depth control is achieved, the process suffers from dry etch induced damage. Selective wet etching suffers from poor recess width control and a residual surface oxide layer after etching which can cause significant variations in the device threshold voltage.

In this paper, we report a non-selective wet chemical digital gate recess etching technique. The process is based on a controlled oxidation/etch technique [3]. The surface roughness was evaluated by both AFM and SEM. In order to assess the uniformity and reproducibility of the process, twenty samples were processed over a six months period. The etch depth uniformity of the samples was also determined by AFM and SEM. This process was then incorporated into a 120nm gate length InP HEMT process. Devices performances at both DC and RF are reported.

WET GATE RECESS ETCH

The new wet etching process is based on the idea of separately controlling the oxidation and de-oxidation of the wet etching process[3]. Normal III-V semiconductor etching occurs by combining two chemical reactions into a single chemical etching system. The semiconductor surface is oxidized by the first chemical reaction and then the oxidised layer is removed by the second chemical reaction. In this gate recess etching process the two chemical reactions were separated into two distinct processes.



(a) Side view (b) Top view

Figure 1. SEM images of 120 nm T gates pattern after recess etch

By choosing appropriate concentration of oxidation solution and optimising the soak time of the sample in the solution, very smooth etched surfaces were achieved. Figure 1 shows SEM images of the recess etched surface with the resist for the deposition of a T-gate still in place. Figure 2 shows AFM images of the recess etched surface after the removal of the resist. By choosing suitable deoxidation

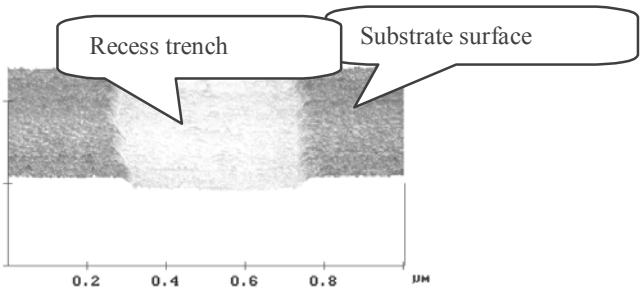


Figure 2. AFM images of gate recess trench after remove resist.

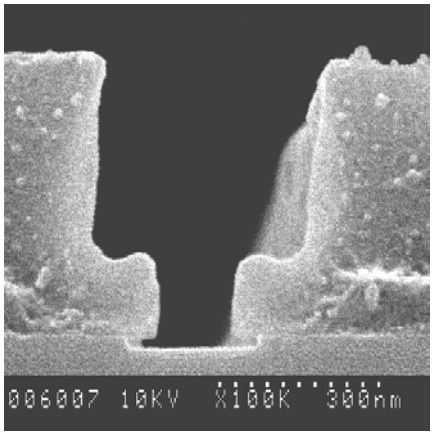


Figure 3 Side view of 120 nm T gate pattern with reduced recess width

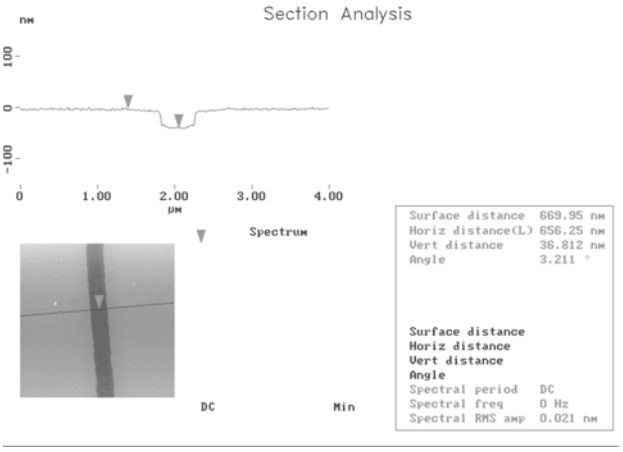
etchant and suitable solution concentration, the recess undercut can also be controlled. Figure 3 show a gate recess etching with reduced recess trench width. The recess trench width shown in figure 1 and figure 2 was about 400 nm, whilst that in figure 3 was about 200 nm. The only difference between the two recess etchings was the concentration of deoxidation etchant used.

In order to assess the uniformity and reproducibility of the process, twenty samples was processed over a six month period. The etch depth uniformity of the samples as determined by AFM and SEM was found to be ±1.5 nm for a 30nm recess etch. Another example demonstrating the uniformity of this etching technology is that the large patterns and small patterns in the same sample were etched at the same rate. (Figure 4)

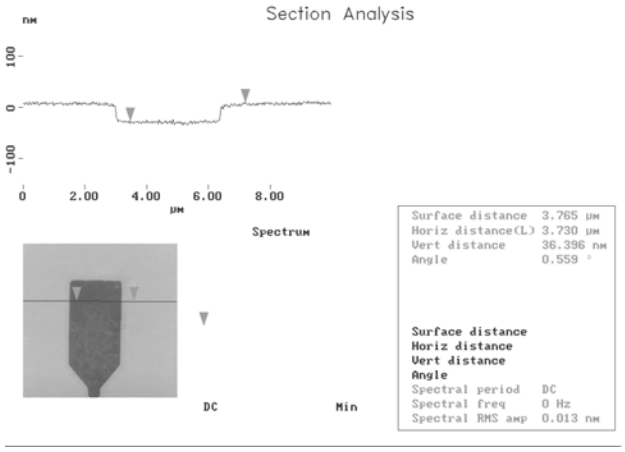
DEVICE FABRICATION AND PERFORMANCE

The devices were fabricated on a Si δ-doped $In_{0.52}Al_{0.48}As/ In_{0.53}Ga_{0.47}As$ lattice matched HEMT structure grown by MBE on an InP substrate. The as-grown room-temperature sheet concentration n_{sh} and Hall mobility μ_H of the structure were $3.0x10^{12}cm^{-2}$ and 9000 cm^2/Vs respectively. Au/Ge/Ni based ohmic contacts with a contact resistance of 0.1 Ω mm were formed prior to mesa isolation using $H_3PO_4:H_2O_2$-based wet etching. T-gate profiles were formed in the 2μm source / drain gap by electron beam lithography using a PMMA/co-polymer/PMMA tri-layer resist. Patterning was carried out using an EBPG5 HR 100 electron beam pattern generator manufactured by Leica Microsystems Lithography Ltd. After wet digital gate recess, the tri-layer Ti/Pd/Au with thickness of 250nm was evaporated to form the Schottky T- gates. Finally, a bond pad with 400nm gold was formed by lift-off to enable the DC and RF characterization of the devices.

The I-V characteristics of gate diode are shown in figure 5 (a). Very low gate leakage current at negative gate bias and a

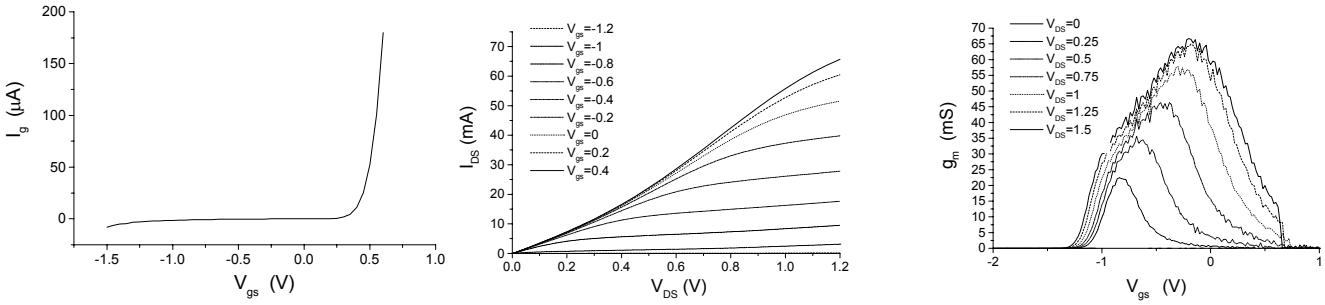


(a)



(b)

Figure 4. AFM images of gate recess trench (a) and gate feed (b). The two measurements were taken on the same wafer. The etch depth difference between the two patterns is only 0.416nm which is within the error of the measurement.



(a) Gate diode (b) I-V characteristics (c) g_m characteristics

Figure 5. DC characteristics of 120 nm gate length 2 x 50 μm gate width InP HEMT devices.

very steep increase of gate current at positive gate bias of 0.5 V suggest that the new wet recess etching does not influence the surface chemistry of etched surface, which is often an issue in selective wet etching recess processes.

The I-V and g_m characteristics of the devices are shown in figure 5 (b), (c). The devices yield on 12mm by 12mm samples containing 112 devices, which mainly depends on gate lithography and gate recess etching, was higher than 95%. We believe this is due to the new gate recess etching technique. The drain saturation current I_{DSS} of 2 by 50 μm gate width devices measured at drain bias of 1 V was 39±2 mA. The pinch-off voltage of the devices on the sample was between –1.1 V and –1.2 V. The uniformity was much better than what has been achieved with others gate recess etching techniques. A g_m of 600 mS/mm was achieved from most of the devices. The best performance devices showed a g_m of 660 mS/mm (figure 5 b).

On-wafer s-parameter measurements were performed from 0.04-60 GHz using an Anritsu 360B Vector Network Analyser and on-wafer Cascade probes utilising ISS calibration. The f_T extracted from the $|h_{21}|$ against frequency was 250 GHz, comparable with the best results we have achieved by other gate recess techniques[4].

CONCLUSIONS

A new non-selective wet etching technique has been developed to etch $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ structure for the gate recess of InP HEMTs. A uniform etch depth and well-controlled undercut width were achieved. In addition, a very smooth etched surface was obtained using this new etching technique. 120nm gate length InP HEMTs devices were fabricated using this new gate recess process. A g_m of 660 mS/mm and f_T of 250 GHz were achieved, performance comparable with the best results we have achieved by using other gate recess technique. Furthermore, the uniformity and reproducibility of the devices was significantly improved.

All the results show that the new recess etching technique provides the same etch depth precision as a selective etch with the additional freedom of not being limited by the vertical layer stack geometry. In addition, this novel etch process utilizes standard wet chemical techniques which do not rely on precisely controlling the temperature and pH of the etching, and so can be easily incorporated into a manufacturing process.

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