A High Performance and High Yield Self-Aligned and Double Recessed pHEMT Process with One Lithography Step for Both Gate and First Recess Definition

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Abstract

A pHEMT device processing method has been developed that allows formation of gate and first recess regions using just one lithography step, resulting in self-alignment of the gate to the first recess. Three stage Q-band power amplifiers with small signal gain of 22-24 dB, saturated output power of 32.4 dBm at Vds=5.0 V, and DC yield of 70 % have been produced. At Vds=6 V, the small signal gain and output power are 20-22 dB, and 33.2 dBm, respectively. The process achieves high performance, high yield, reduced complexity, and reduced cost simultaneously.

Key Word: Self-aligned, pHEMT, Double Recessed

INTRODUCTION

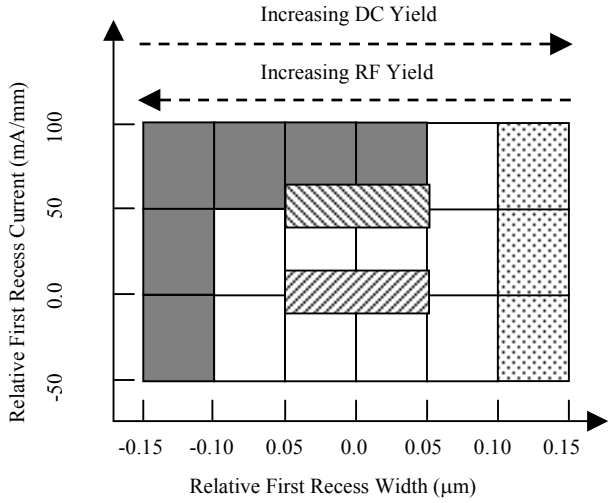
Double recessed pHEMT and HFETs are widely used for RF power amplifiers from L band to Q band [1-2]. At Ka band and beyond, high performance amplifiers require tight control of the alignment between the first recess and gate. On one hand, too large of a first recess deteriorates the output power. On the other hand, too small of a first recess causes parametric breakdown failure. The tradeoffs between the DC yield, RF yield, and first recess current have been discussed in [3] and are shown in Figure 1. A method that would remove the alignment tolerance constrains between the first recess and gate in a double-recessed power amplifier technology is highly desirable.

Self-aligned ion implanted MESFET devices using W based refractory gates, such as TiWN or WSiN have been reported in the past [4]. This technology has been extended to hetero-structure FETs as well [5]. However, the ion implanted refractory based self-aligned gate technology requires high temperature annealing for implant activation. The annealing temperature and time are usually determined by a compromise between the acceptable activation efficiency of the implanted ions and the degradation of various hetero-interfaces and the FET channel mobility. Furthermore, a separate lithography step is required to form a low resistance Au metal strap (Tee-top) to the W based gate in order to reduce the gate resistance to an acceptable value for RF amplifier application.

In this paper, we describe a method that would bring the benefits of self-aligned gate structure to the standard double recessed pHEMT and/or HFET devices without adding processing complexities. In fact, the proposed method reduces one processing step altogether.

SELF-ALIGNED pHEMT/HFET BASIC PROCESSING METHOD.

A schematic cross sectional view of a double recessed self-aligned FET structure is shown in Figure 2.



Best Power, Gain , and DCxRF Yield
Nominal Power and Gain and Best DCxRF Yield
Good Power and Gain
Low (-1 to –2 dB) Power and Gain

Figure 1. Illustrating process sensitivity and yield trend for a Q band power amplifier process. Data is from Ref. [3].

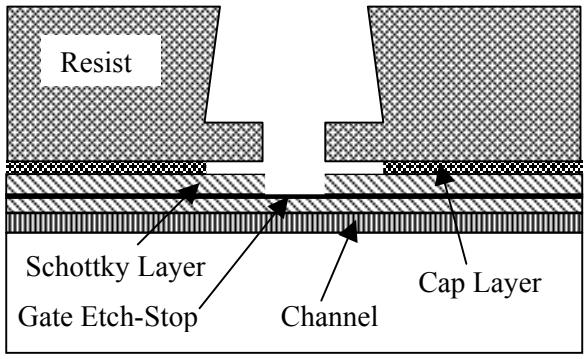


Figure 2. A generic cross-sectional schematic of a double-recessed and self-aligned pHEMT device.

a.) Referring to Figure 2 and following device isolation and ohmic contact formation, the Tee-gate is patterned using standard lithographic techniques [3]. Next, a gate etch solution (type 1) is used to etch the cap layer and the Schottky layer and stop at the gate etch stop layer. For an InP based HEMT device, the cap layer could be InGaAs, and the Schottky and etch stop layers might be InAlAs, and AlAs, respectively. For a GaAs based pHEMT device, the cap layer could be GaAs or InGaAs and the Schottky layer could be InGaP or AlGaAs. The etch stop layer could be InGaP or AlAs. It is important for the gate etch solution (type 1) to etch both the cap layer and Schottky layer at practically equal rates. However, the etch rate selectivity of etch stop layer, with respect to the cap or Schottky layer, in type 1 etch solution should be very high. Citric acid based etch solutions published in the literature [6] can satisfy these requirements.

b.) A second etch solution (type 2) selectively etches the cap layer in the lateral direction. The Schottky and gate etch-stop layers have a very high etch selectivity compared to the cap layer. Citric acid based etch solutions reported in the literature can satisfy these requirements [6]. This etch step defines the first recess, which becomes self-aligned to the gate. The distance between the edge of the gate and first recess on the drain and source side can be controlled from 0.05 μm to several tens of microns.

c.) Finally, the gate metal is evaporated and lifted off. The resulting FET structure is self-aligned, i.e.; there is no misalignment between the gate and the first recess. The other advantage of this process is that just one lithography step is used for the definition of both first recess and gate. Consequently, the first recess lithography step has been eliminated. Therefore, this processing method can achieve high performance, high yield, reduced processing complexity, and reduced cost simultaneously.

A cross sectional view of a Ti/Pt/Au self-aligned pHEMT device is shown in Figure 3.

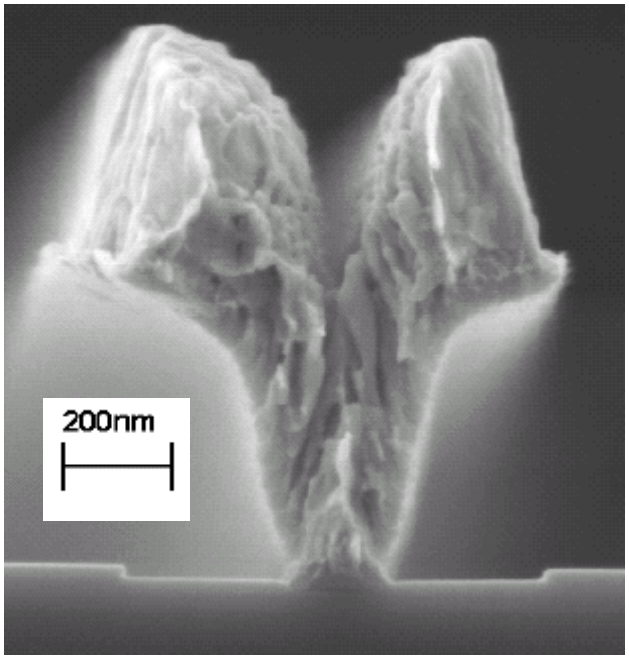


Figure 3. SEM cross-sectional view of a double-recessed self-aligned gate GaAs pHEMT device.

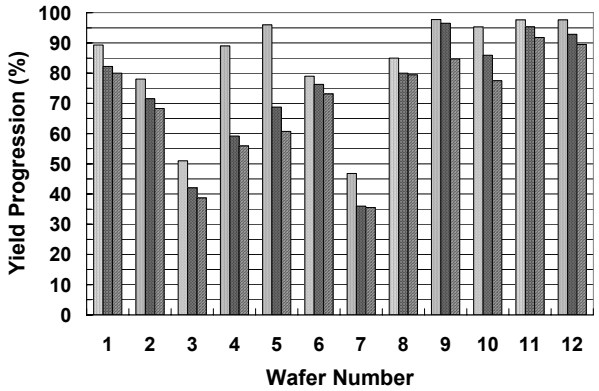


Figure 4. Illustrating parametric yield for individually grounded backside via holes, 1 mA/mm breakdown voltage (Vbdg1), and pinchoff voltage at 1 mA/mm drain current.

DEVICE RESULTS AND YIELD

The self-aligned processing method was applied to the fabrication of Q-band amplifiers [3]. DC yield from twelve wafers is shown in Figure 4. The average yield is 70% for a circuit with >8.0 mm gate periphery. Yield loss in two wafers was tracked to the mis-alignment of via holes in the individually grounded source vias. Excluding these two wafers, the DC yield would be 76%. RF performance of several chips is shown in Figure 5. The saturated output power of the chips shown in Figure 5 tracked within a few tenth of a dB. The average output power and power added efficiency over the band of interest is 32.4 dBm and 25% at Vds=5.0 V. The corresponding values for Vds=6.0 V are 33.2 dBm and 23.7%, respectively.

CONCLUSIONS

A method for fabricating high performance, high-yield, double-recessed and self-aligned pHEMT devices has been developed. The process is compatible with standard Ti/Pt/Au gates and liftoff technique. It provides one with the ability to control the distance between gate and source/drain edges of

the first recess from 0.05 um to several tens of microns. A further benefit is elimination of the first recess lithography step. We believe this process will become the preferred method for fabrication of power amplifiers at Ka band and higher frequencies.

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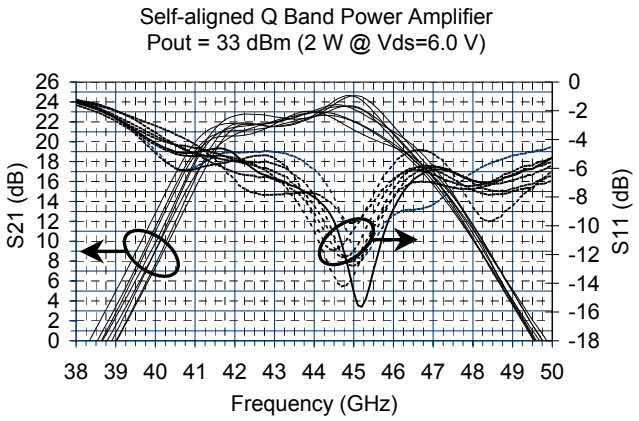

Figure 5. Illustrating the performance of a double-recessed, three-stage Q band power amplifier produced with the self-aligned process.

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List of Acronyms

MESFET: Metal semiconductor field effect transistor
pHEMT: Pseudo-morphic high electron mobility transistor
HFET: Heterojunction field effect transistor
TiWN: Titanium tungsten nitride
WSiN: Tungsten silicon nitride
Ka Band: A designated frequency range of 26.5 to 40.0 GHz
Q Band: A designated frequency range of 33.0 to 50.5 GHz

