Electrophoretic Photoresist Application for High Topography Wafer Surfaces

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ABSTRACT

As wafer surfaces become topographically more challenging, achieving uniform resist coatings in deep vias, over high mesas, and three-dimensional (3-D) features may no longer be possible using conventional, solvent based, spin-coated liquid photoresist (LPR). Thinning of the resist on the high areas and pooling of the resist in the deep areas are common problems. Electrophoretic photoresist (EPR) may be used to achieve conformal 3-D resist coverage over high topography regions, while maintaining the high resolution and wet etch resistance properties of spin-coated LPR. Also, EPR may offer a higher throughput than spin-coated LPR.

This presentation will describe two distinct applications where conformal masking of high topography wafer surfaces is needed and achieved by using EPR. The first application involves a silicon-on-glass (SOG) device technology that requires conformal masking of retrograde silicon pedestal structures up to 170 μm high. The second application is for GaAs wafer through substrate via holes. For high power GaAs devices, a solder-stop metal needs to be masked inside the via to prevent Au-Sn eutectic solder from wicking into the hole during the solder die attach step.[1, 2]

INTRODUCTION

The application of spin-coated LPR to a wafer surface with minimal topography results in a layer of fairly uniform thickness. However, this technology can fail dramatically in the coverage of highly elevated structures or deeply etched grooves that obstruct the even spread of the spin-coated LPR across the wafer surface. The uniformity of the spin-coated LPR layer depends upon the topography of the wafer surface, the fluid flow dynamics, and the resist properties including viscosity and vapor pressure. Spinning the wafer generates centrifugal forces that force the LPR to flow towards the wafer perimeter. When these forces exceed the surface tension at the wafer perimeter, excess LPR escapes. These forces are dependent upon topography and vary considerably within holes and on mesa sidewalls in comparison with flat surfaces. This can result in a substantial resist coat thickness variation from substrate center to edge. Effects include severe resist thinning on mesa sidewalls and tops of elevated features and the pooling of resist inside deeply etched via holes. In extreme cases the LPR may "skip over" or "tent" high aspect ratio via holes without filling them

To overcome the limitations of using spin-coated LPR on wafer surfaces with extreme topography, several alternative methods have been introduced to wafer fabrication in recent years. These methods include silk-screen printing and spray-dispense coating, which are used for electronic packaging and some printed circuit board (PCB) applications. A meniscus coating process, which is used for flat panel display substrates, has also been investigated. Another interesting technique is the deposition of solid polymer from the gas phase. This method requires a monomeric coating material, which is evaporated at ambient temperatures and coalesces into polymeric form onto the substrate surface. Finally, ultrasonic spray coating is a relatively new technique for the deposition of a uniform photoresist layer on extreme 3-D topography wafers, such as MEMS (micro-electromechanical systems).[3-5] This technique utilizes an ultrasonic atomizer, which generates an aerosol of small droplets, and these droplets stay where deposited, allowing for a fairly uniform resist coating to be achieved across the 3-D topography wafer.

EPR was introduced to the PCB industry over a decade ago, and it enabled conformal photoresist coverage on highly irregular shaped surfaces, such as via holes.[6-11] Over the past few years, a number of papers have been published on the use of EPR for wafer processing applications, such as MEMS, sensors, high topography optical components, and wafer level packaging.[11-16] A thin conductive seed layer is required on the substrate surface, and the deposition process is very similar to electroplating. Conventional substrate plating tool platforms can be adapted for EPR by adding a continuous ultra-filtration, closed loop system and permeate rinse bath.[9,11,12,14,15] The EPR process deposits a conformal, chemically resistant photoresist layer on an exposed, conductive surface through migration of an organic polymer to an electrically charged electrode.[6-11,15] It involves the migration of charged micelles in solution toward the oppositely charged electrode (substrate). Micelles are colloidal particles containing active photoresist constituents, which are the polymer, photoactive compound (PAC), solvents, and dye. The process can be anodic or cathodic. Electrodeposition of the photoresist consists of three steps: electrophoresis, electrolysis, and electro-osmosis.[11] After the substrate is immersed into the EPR bath, a high voltage is applied between the conductive seed layer and a counter electrode for several seconds, which results in the deposition of resist onto the seed layer. The deposited resist is non-conductive, so a large potential gradient is built up across the resist film. This leads to decrease in the current flow until

electrolysis stops (current reaches zero). This self-limiting behavior results in a highly conformal film electrodeposited from an aqueous emulsion solution on the order of 4-18 µm.[11-14,15] The final thickness is dependent upon the bath contents of a special thickness controlling (TC) chemical, the bath temperature, and the applied voltage.[11-14,15] After deposition the wafer is rinsed, dried, and then baked causing the compacted micelles to level into a smooth continuous layer of resist.

APPLICATIONS

The 170 µm high pedestal structures, as shown in Figure 1 on silicon wafers, provide the basis for heterolithic microwave integrated circuit (HMIC) processing.[17] Some HMIC designs require a highly conductive metal scheme, such as sputtered Ti/W-Ag-Ti/W, to be deposited over the pedestal region. This metal scheme is not self-aligning and selective removal of the metal from the top center of the pedestal region is desired. A conformal resist mask is required in order to protect the metal films on the pedestal top perimeter edge, sidewalls, and base during the subsequent wet etch step. The silicon pedestals can be fabricated utilizing a wet, anisotropic etch process[17], which results in sidewalls parallel to (111) planes and 55° sidewall angles, or an inductively coupled plasma (ICP) etch, which produces slightly retrograde sidewall profiles (see Figure 1).

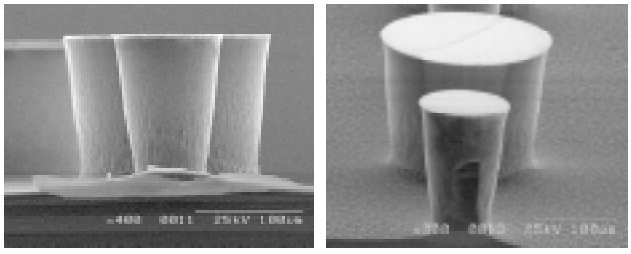


Figure 1: 170 µm high Si pedestal topography produced by an ICP etch. The slightly retrograde sidewalls require a conformal resist coat that also covers the pedestal top perimeter.

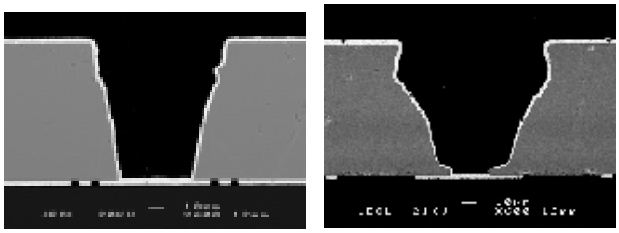


Figure 2: GaAs vias produced by reactive ion etching (RIE) using BCl_3/Cl_2 chemistry. The two via cross sections shown were cleaved and polished in perpendicular directions. Conformal resist mask coverage is desired over the sidewalls including the retrograde portion.

For high power GaAs devices, a positive photoresist mask is used to cover solder-stop metal inside the via holes while this metal is wet etched from the back-side leaving an inert Au surface for subsequent Au-Sn eutectic solder die attach. The oxidized solder-stop metal lining the via sidewalls prevents Au-Sn from the solder pre-form from wicking into the hole during die attach.[1,2] The holes can be up to 100 µm deep as shown in Figure 2. For low aspect ratio vias, a thick, positive LPR has been successfully used for the past several years. Recently, there has a been a strong effort to reduce via size and increase aspect ratio, which can result in a coverage problems when trying to use LPR.[1,2] EPR can be used to address this issue.

EXPERIMENTAL & RESULTS: HMIC Si PEDESTAL STRUCTURES

Five 100 mm diameter Si wafers with pedestals fabricated using a wet, anisotropic etch process were sent to Semitool, Inc. for coating with PEPR™ 2400 photoresist[18], which is a positive EPR with negatively charged micelles available from the Shipley Company. The PEPR™ 2400 was deposited in a Semitool semiautomatic, single wafer ECD (electro-chemical deposition) platform fitted with an EPR reactor.[11] The deposition parameters, such as temperature, filtration, voltage, current, and the PEPR™ 2400 TC plasticizer concentration were maintained at Semitool's process of record conditions. The wafers, which were held horizontally with the Ti/W-Ag-Ti/W layer facing downward in the ECD chamber, were rotated during the deposition process, which took less than 2 minutes per wafer. After deposition the wafers were baked on a hotplate at about 100°C for 10 min to remove moisture from the film and smooth the film surface. Conformal PEPR™ 2400 coatings over the 170 µm high pedestals covered with the Ti/W-Ag-Ti/W layers were achieved on all five wafers.

The wafer surfaces were inspected using a SEM (scanning electron microscope), and coat uniformity appeared to be excellent including the sidewall, top, and edge coverage. The deposited resist layer had a uniform and shiny appearance on all five wafers. Figure 3 shows SEM images of the PEPR layer covering the underlying structures. Smooth, continuous coverage of resist film was achieved over all of the analyzed features. About 70% of the average thickness was maintained over even the most challenging feature, a square topped plateau with sharp outside corners. Typical coverage over convex corners is slightly thinner than the average thickness because of rounding that occurred during the bake step.

Alignment and exposure were carried out on a Canon PLA-501F broadband contact/ proximity mask aligner. Instead of using the Shipley recommended sodium carbonate developer with Photoposit 7412 Defoamer[18], 0.26 normal MIF developer, which is TMAH (tetra-methyl ammonium hydroxide) based, was used. The developed areas were completely open, but the sharpness of the resolved pattern was not optimized.

The wafers were then subjected to a Ti/W wet etch composed of hydrogen peroxide and EDTA (ethylene diamine tetra-acetic acid) at room temperature (RT), but the etch did not initiate even though it was compatible with the PEPR mask. Microscopic inspection did not reveal any

obvious clues concerning etch initiation. At first resist scum or a monolayer organic film was suspected to be preventing etch initiation. A couple wafers were stripped free of the PEPR and immersed in this wet etch solution. The previously shiny Ti/W film now had a dull brownish appearance. Auger surface and depth analysis showed strong signals for Ti and O at and near the film surface. Titanium oxidizes more readily than other metals, and the surface of the Ti layer was anodized during the EPR deposition process. In this case oxidation of the seed layer occurred in addition to the electrolysis reaction. A 30 sec buffered oxide etch (BOE containing HF) was found to etch through the Ti oxide layer, so that Ti/W etch could be subsequently used after a quick de-ionized (DI) water rinse. The Ag was also etched by the RT hydroxide peroxide/ EDTA solution.

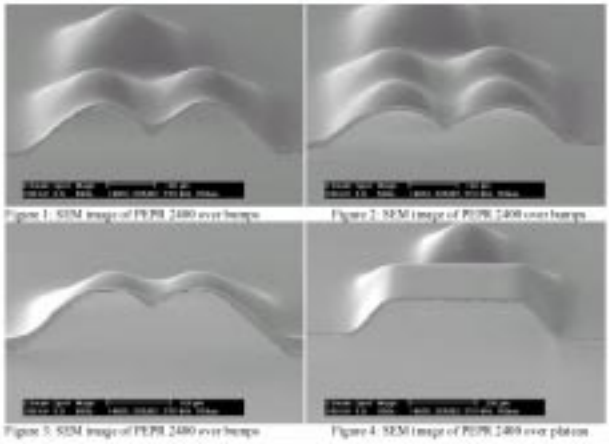


Figure 3: SEM images of PEPR™ 2400 coverage of wet etched pedestals.

The second iteration of this investigation will involve depositing PEPR™ 2400 over Si pedestal structures with slightly retrograde sidewalls prepared using ICP (see Figure 1). EPR deposition may be the only method that ensures 100% resist coverage of the retrograde sidewalls because it does not have line of sight limitations.

EXPERIMENTAL & RESULTS: GaAs THROUGH SUBSTRATE VIAS

At M/A-COM two sets of GaAs wafers were mounted on sapphire carriers with Staystik 336T thermoplastic temporary bonding adhesive. The backside thinning (100 µm), via etch, and electroplate steps have been described previously.[1,2] The high aspect ratio vias had a backside surface opening of about 90 µm and a front-side opening adjacent to the bond pad of about 50 µm (see Figure 1).[2] After the etch, photomask strip and clean, and electrodeposition steps, a blanket electroless Ni/P solder-stop layer (very low P content, ≈0.1 µm) was deposited onto the backside, 3.0 µm thick electroplated gold layer using a dilute $PdCl_2$ based catalyst solution.[1,2]

At Semitool the PEPR™ 2400 was deposited onto the electroless Ni/P solder-stop layer (anode) utilizing the Equinox ECD platform with the wafer holder adapted for the thicker sapphire carriers. Prior to deposition the electroless Ni/P solder-stop layer was immersed in a RT 1 HCl: 1 H_2O solution to remove the surface oxide layer. During the deposition the thin wafer/ carriers were rotated to improve uniformity and help prevent oxygen gas generated during the electrolysis reaction from becoming trapped inside the vias. After deposition the samples were baked on a hotplate as previously described.

Prior to the exposure and develop steps, the deposited PEPR film thickness could not be measured. Using a Suss MA150 i-line (365 nm) backside contact/ proximity mask aligner, it was determined that a dose of 2000 mJ/cm^2 (50 mW/cm^2 for 40 sec) provided sufficient exposure through the PEPR film. A backside dice street mask was used for the exposure experiment. To clear the exposed PEPR, a 3 min RT, immersion develop with agitation was done using a TMAH based developer. The developed areas were de-scummed in an oxygen plasma generated within a barrel asher. A Tencor P-11 surface depth profiler was used to measure the resist thickness at five points (near major flat, near minor flat, center, opposite major, and opposite minor) across several of the wafers on the backside surface using the open dice streets. The average PEPR thickness per wafer ranged from 9.5-10.5 µm with a TTR (total thickness range) across an individual wafer of approximately 3µm.

After de-scum the Ni/P was removed from the dice streets using a RT, dilute ferric chloride wet etch (compatible with PEPR) for approximately 45 sec as shown in Figure 4. The very thin Pd catalyst layer was then removed using a concentrated sulfuric acid/ hydrogen peroxide mixture (1 H_2SO_4: 1 H_2O_2: 3 H_2O) at RT for 15 sec. Unfortunately, the resist mask was attacked and undercut during this etch step as shown in Figure 5. Klocke and Steeper previously showed that PEPR™ 2400 can stand up to a dilute sulfuric acid/ hydrogen peroxide mixture used to etch a sputtered copper seed layer.[11] The gold was then removed from the dice streets using a RT KI/I_2 based etch solution compatible with the PEPR mask.

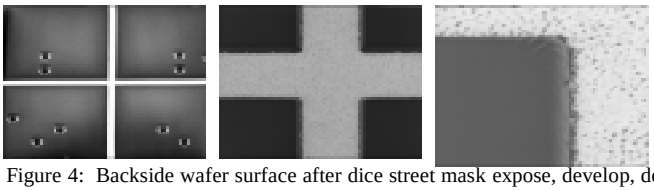


Figure 4: Backside wafer surface after dice street mask expose, develop, de-scum, and dilute ferric chloride etch. The light areas are exposed metal (Pd spots on Au) and the dark areas are the PEPR™ 2400 mask.

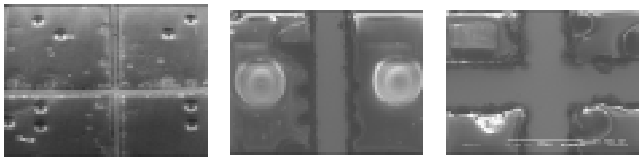
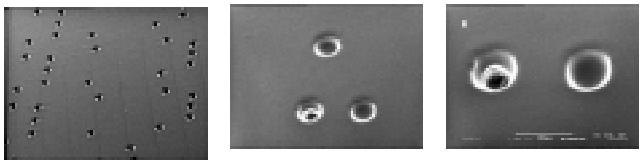


Figure 5: Backside wafer surface after RT, 15 sec 1 H_2SO_4: 1H_2O_2: 3 H_2O immersion etch to remove Pd. Au is shown within the dice streets. The dark PEPR mask areas have been attacked & undercut by the etch solution.

The goal of this evaluation was to determine if PEPR™ 2400 could be used to replace the thick LPR for covering the high aspect ratio via sidewalls. The sidewalls need to be covered when the dice streets are etched and also when the solder-stop Ni/P layer is removed from the backside surface leaving an exposed electroplated gold layer for Au-Sn eutectic solder die attach. It may be possible to utilize a more dilute sulfuric acid / peroxide mixture to remove the very thin Pd catalyst layer without attacking the PEPR. Also, most GaAs power device wafer facilities use either sputtered Ti or Ti/W for the solder-stop layer, and the PEPR has been shown to be compatible with some wet etch solutions for these two types of solder-stop layers.

In addition to the etch undercut issue, we observed pinholes in the deposited PEPR™ 2400 film within some of the vias as shown in Figure 6. For all of the wafers, over 95% of high aspect ratio vias from across the experiment wafers showed excellent conformal coverage. Most of the pinholes appeared to be concentrated near the center of the backside surface. Wafer rotation effectively removes gas bubbles from the outer edges of the wafer. Bubbles and the resulting pinholes on a substrate surface typically result from contamination or poor wet-ability of the underlying conductive layer. Electrophoretic photoresist processes are sensitive to the surface properties of the substrate. Semitool has demonstrated pinhole free depositions on other substrates. With further optimization of precleaning and deposition procedures, pinhole free coatings should be attainable for GaAs wafer backside via applications as well.



(a) PEPR covering all vias (b) 1 pinhole, 2 good (c) 1 pinhole, 1 good

Figure 6: Pinholes noted within some backside vias. The pinholes may have been caused from gas bubbles trapped within the vias.

CONCLUSION

Shipley PEPR™ 2400 is a positive, i-line EPR that is compatible with contact/ proximity mask alignment and exposure systems. The developer and stripper are different than what is currently used for wafer spin-coated LPR, but it is commercially available and can be easily integrated into a wafer facility. The deposition tool is slightly more complex than a conventional electroplating system. However, a commercialized system and process is available from Semitool, Inc.[19]

The PEPR process delivered excellent conformal coatings with very uniform thickness, including on the sharp top edge of the Si pedestals. The thickness is self-limiting and appeared shiny and without pinholes. PEPR was also found to be a promising candidate for masking high aspect ratio through wafer vias for the GaAs application. The via walls could be masked, and the dicing streets could be defined for subsequent wet etch steps. However, this positive, anodic EPR was found to be incompatible with a concentrated sulfuric acid/ hydrogen peroxide etch solution used for the thin Pd catalyst layer removal. Further development is needed for a Pd etch chemistry that is compatible PEPR™ 2400.

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