AlGaN/GaN HEMTs on Silicon Carbide Substrates for Microwave Power Operation

Richard Lossy[1], Nidhi Chaturvedi[1], Peter Heymann[1], Klaus Köhler[2], Stefan Müller[2] and Joachim Würfl[1]

[1]Ferdinand-Braun-Institut für Höchstfrequenztechnik, Albert-Einstein-Straße 11, 12489 Berlin, Germany
[2]Fraunhofer-Institut für Angewandte Festkörperphysik, Tullastraße 72, 79108 Freiburg, Germany
Phone: +49 30 63922630 Fax: +49 30 63922685 e-mail: lossy@fbh-berlin.de

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ABSTRACT

Results from technology and microwave characterization of large periphery AlGaN/GaN power HEMTs on insulating SiC substrates are presented. The influence of processing steps on device performance is discussed. DC characteristics reveal current densities above 1.2 A/mm and extrinsic transconductances of 275 mS/mm. A power density of 5.2 W/mm @ 2 GHz is obtained for devices up to 2 mm gate width. The maximum power level achieved on-wafer is 13.8 W @ 2 GHz for 4 mm wide devices. A hybrid amplifier using packaged 4 mm devices delivers 15.1 W.

INTRODUCTION

As promising candidates for future microwave power devices, GaN-based high-electron mobility transistors (HEMTs) have attracted much research interest. Their potential is due to advantageous material properties such as the wide band gap leading to high breakdown voltage and high saturated-electron drift velocity. Also, the existence of AlGaN/GaN heterostructures with high conduction band offsets in combination with the spontaneous polarization effect results in high sheet carrier densities in the 1×10^{13} cm^{-2} range. Furthermore, SiC as a substrate material provides an excellent thermal conductivity, comparable to copper. This is mandatory for effective heat removal in high power applications. All these features together account for devices with very high absolute microwave output power levels.

TECHNOLOGY AND DC CHARACTERISATION

The $Al_{0.25}Ga_{0.75}N$/GaN HEMT structures were grown in a multiwafer MOCVD (6x2") reactor yielding high throughput and reproducibility. Device fabrication was accomplished using i-line stepper lithography. However, without certain technological precautions the transparency of SiC-wafers with AlGaN/GaN epitaxy impedes a precise and reliable image alignment with respect to wafer surface and orientation. Therefore, special processing sequences were developed to allow the proper exposure. A sophisticated metallization scheme was employed for fabrication of the ohmic contacts that preserves pattern delineation during rapid thermal annealing at 830°C [1-3].

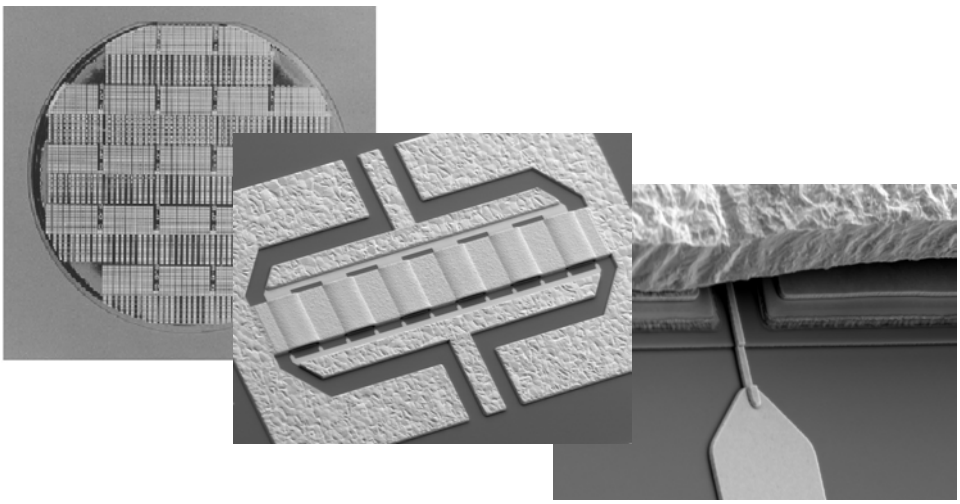

Fig. 1: AlGaN/GaN HEMTs on a 2" wafer (left) comprising parallel transistor fingers (center) and detail of the gate feeding (right) also showing the transistor channel and arch of the air bridge structure.

Gate contacts were made using Pt/Au metallization. A gate length of 0.5 µm was defined with stepper lithography, shorter gate lengths down to 0.25 µm were defined by electron beam lithography (ZBA23-40kV). Large devices with different gate widths ranging up to 4 mm were fabricated using an air bridge technology (Fig. 1).

In order to optimize thermal and electrical properties, power cell design variations have been integrated on chip. Different scaling strategies regarding the number and width of the gate fingers or the gate pitch, i.e. spacing between repeating cell structures have been implemented.

DC measurements revealed a saturated drain current of I_{DSS}=1.2 A/mm (V_G= +2V). Due to the excellent contact resistance (0.3 Ωmm), the source-gate resistance is 0.85 Ωmm. This leads to a calculated intrinsic $g_{m,max}$ of 360 mS/mm (extrinsic 275 mS/mm) and an on-resistance of R_{on}= 2 Ωmm.

THERMAL SIMULATION

Thermal simulations were performed using a three dimensional finite-element model in the Nastran-Patran software package. The goal was to extract optimized device designs for a given packaging technique. The GaN chip dimensions used for simulation were 1.5×2 mm² with a device layout using parallel gate fingers. The active element of heat dissipation was represented by a 2-D planar heat source at each of the gate fingers. For better comparison, the different device geometries used the same dissipated heat per gate width (5 W/mm).

The chip package was a standard CuW RF power transistor package with a thermal conductivity of 180 W/mK. For die attachment a Au/Sn eutectic solder was used.

The largest device with a total of 4 mm gate width consisted of 16 gate fingers each having a width of 250 µm (referred to 16x250). The distance between the individual gate fingers was 50 µm pitch for most transistors.

Table 1 compares the simulation results of the different geometries. The following conclusions can be drawn:

1) Using SiC-substrates the temperature rise is not higher than 120°C for all geometries under consideration.

Table I:
Maximum Device Temperature

Device Size	Chip Package	Gate Pitch	Substrate	T_{max} /°C
16x250	✓	50	SiC	143
16x250	✓	100	SiC	113
16x250	*	50	SiC	92
8x125	*	50	SiC	77
16x250	*	50	Sapphire	679

* chip without housing fixed on base plate
Simulated maximum device temperatures for different transistor geometries and substrates: Base plate temperature held at To=27°C.

2) A gate pitch of 50 µm is sufficient to achieve tolerable device temperature.
3) The thermal resistance of the chip package cannot be neglected.

PASSIVATION

For AlGaN/GaN-HEMTs it is known that the maximum power levels under rf-operation degrade substantially compared to the expectations based on DC measurements. This degradation could be reduced significantly if the HEMT surface is passivated. As an example the rf-power recovery after passivation is given in Fig. 2, where the passivated HEMTs show an average increase of the maximum rf-power by a factor of 3 after passivation using SiN_x.

According to the general understanding this improvement is mainly due to a reduction of electrically active surface traps. However, due to the effect of spontaneous polarization on the 2DEG carrier concentration, the mechanical strain of the passivation layer might influence device performance. We checked this by comparing tensile and compressive types of SiN_x

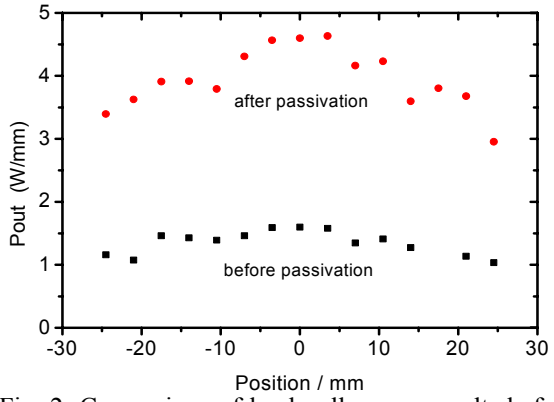

Fig. 2: Comparison of load pull power results before and after passivation for HEMTs at different radial position on the wafer. The gate width is 100 µm.

passivation layers. No differences in the rf-power after passivation could be found.

The recovery of the rf-power after passivation is substantial, but far not complete. This can be demonstrated by pulsed I/V-measurements of the passivated devices. The related mechanisms are generally referred to as the gate-lag and drain-lag phenomena [4, 5]. The gate-lag phenomenon is associated with traps in the vicinity of the gate, the drain lag phenomenon is related to backgating effects due to electron trapping in the buffer layers [5].

Pulsed measurements on passivated devices as shown in Fig. 3 visualize these trapping effects. During pulsing the gate and drain voltage

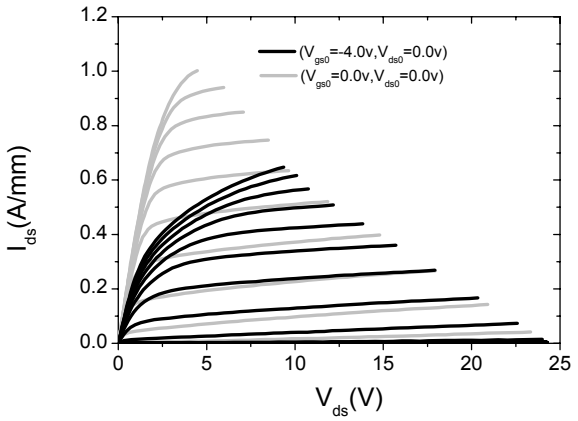

Fig. 3a: Pulsed measurement of I/V-characteristics:
Steady bias points:
V_{GS} = 0 V; V_{DS} = 0 V
V_{GS} = -4 V; V_{DS} = 0 V
gate voltage sweep: -4 V .... +1 V

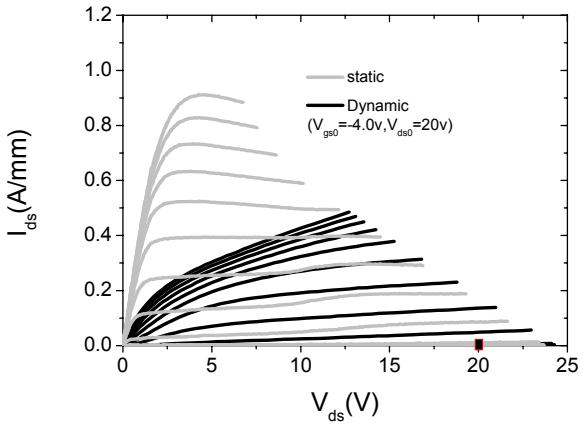

Fig. 3b: Comparison of static ( ) and dynamic ( ) output characteristics. Steady bias point for pulsed measurement:
V_{GS} = -4V; V_{DS} = 20 V
gate voltage sweep: -4 V .... +1 V

is switched simultaneously away from a steady bias point to the point where the current had to be measured for a very short time (pulse length: 0,2 µsec, pulse separation 1 msec). Therefore trapped electrons and holes cannot follow these fast changes. They are "frozen" at those biasing conditions where the pulsing starts from.

The measurement conditions according to fig. 3a highlight the influence of traps in the vicinity of the gate space charge region (gate-lag). At the steady bias point of V_{GS} = 0V and V_{DS} = 0V practically no traps are activated since the gate space charge region is very small. Pulsing from these conditions nearly represents the ideal I/V- characteristics as it would appear in the absence of any traps. However, for a steady gate bias close to pinch off the gate space charge region is expanded, therefore traps in the vicinity of the gate, especially at the surface are activated. The corresponding pulse measurements reflect these conditions as shown in fig. 3a (black curves).

If the steady bias point of the drain source voltage (V_{DS}) is set to higher values (fig. 3b, black curves) these measurement conditions additionally consider the effect of traps located in the buffer (drain-lag). Due to the band bending resulting from this bias point also traps in the buffer are activated, leading to dynamic conditions as shown by the black curves. If the device is biased at large signal microwave conditions the effectively usable I/V-characteristics is close to these conditions. For comparison the static I/V-characteristics is also given in fig. 3b (gray curve). The difference between these curves clearly demonstrates further potential of improvements if material quality and processing is optimized accordingly.

MICROWAVE CHARACTERISTICS

S-parameters of the microwave power transistors were measured up to 50 GHz. For the L_G=0.3 µm gates a current gain cut-off frequency f_t of 37 GHz was obtained. Therefore, the L_G x f_t product is 10 GHz µm. This compares well with the 0.5 µm gates for which we measured f_t =21 GHz. Devices having 100µm gate width reveal f_{max}= 74 GHz. For larger devices (gate width 4 mm, L_G= 0.3 µm) f_{max} reduces to 31 GHz.

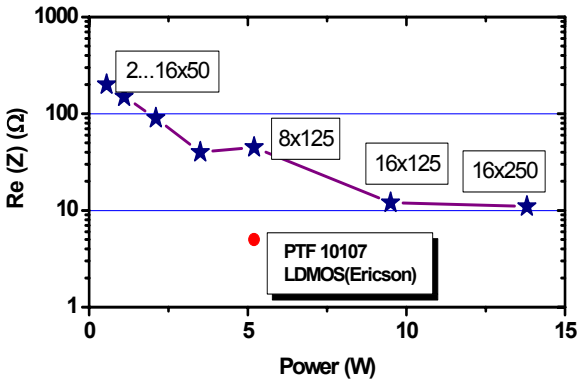

Fig. 4: Scaling of the output impedance with gate width at 2 GHz. The insets indicate the number of transistor fingers times finger width.

Large signal on-wafer microwave measurements were made at 2 and 10 GHz using passive load-pull systems in class A operation. For a device with a gate width of 4 mm (16x250µm) the maximum output power of 13.8 W @ 2GHz could be achieved. The corresponding efficiency (PAE) was 53 %, gain is 25 dB and decreased to 21 dB in saturation. The highest power density measured was 5.2 W/mm and could be obtained on devices ranging from 100 µm width up to 2 mm. 4 mm wide devices deviate from this linear scaling and in this case the output power was reduced to 66 % of the expected value. Load-pull measurements at 10 GHz reveal a maximum power density of 4.5 W/mm. This slight reduction may be explained by device parasitics at higher frequencies.

The large signal output impedance at 2 GHz was calculated from the Γ-load values of the load pull measurements. The results for devices up to 4 mm gate width are given in Fig. 4, showing a scaling with device size and thus device power. For a given power level of 5 W the output impedance of GaN-devices by far exceeds that of their LDMOS counterparts. High output impedances are favorable for combining power cells to high power microwave amplifiers.

POWER AMPLIFIER

Transistors of 4 mm gate width were diced and packaged in a commercial CuW-package using AuSn chip-bonding. The packaged devices were mounted in a single stage amplifier designed for operation at frequencies of 1…2.5 GHz at 50 Ω (Fig. 5). The maximum output power in this configuration is 41,8 dBm (15,1 W) at 2 GHz.

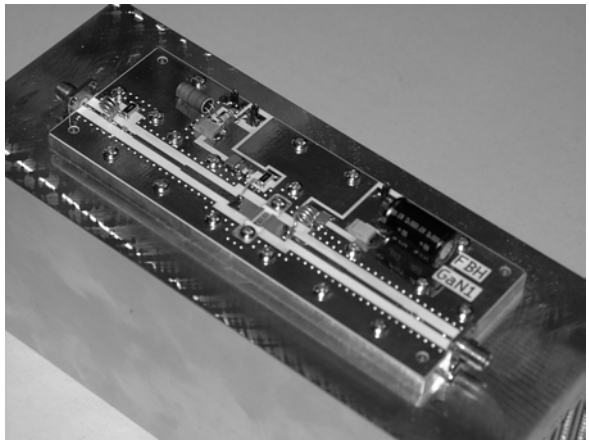

Fig. 5: Single stage amplifier with GaN-power HEMT

CONCLUSION

A technology based on stepper lithography was developed for the fabrication of large AlGaN/GaN HEMTs on SiC substrate. Devices of different size with a gate width up to 4 mm were characterized. DC characterization yielded a saturated drain current of 1.2 A/mm and an intrinsic transconductance of 360 mS/mm. Load-pull measurements were performed at 2 and 10 GHz. From these devices a power density of 5.2 W/mm was achieved at 2GHz. The maximum power level obtained was 13.8 W for a 4 mm wide device, showing a power gain of 25 dB.

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REFERENCES

[1] R. Lossy, N. Chaturvedi, J. Würfl, St. Müller, K.Köhler, physica status solidi (a)Vol.194 (2), 2002.pp.460-463.

[2] R. Lossy,. J. Hilsenbeck, J. Würfl, K. Köhler and H. Obloh, Proc. Int. Workshop on Nitride Semiconductors 2000, IPAP Conference Series 1, p942-945

[3] J. Hilsenbeck, E.Nebauer, J. Würfl, G. Tränkle, and H.Obloh, El.Lett. 36, 981(2000)

[4] S. C. Binari, K. Ikossi, J.A. Roussos, W. Kruppa, D. Park, H.B. Dietrich, D.D. Koleske, A. E. Wickenden, R.L. Henry, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs" IEEE Trans. on Electron Devices, vol. 48, no.3 pp. 465-471, March 2001

[5] S. De Meyer, C. Charbonniaud, R. Quere, M. Campoveccio, J, Würfl, R. Lossy, "Mechanism of power density degradation due to trapping effects in AlGaN/GaN HEMTs", paper accepted for presentation at the 2003 International Microwave Symposium, Philadelphia, USA

