Transition of High Power SiC MESFETs from 2-inch to 3-inch Production for Improved Cost and Producibility

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Abstract

Significant progress has been made in the development of 3-inch High Purity Semi-insulating (HPSI) 4H-SiC substrates and associated SiC epitaxy. Micropipe densities as low as 4.7 cm^{-2} have been demonstrated for 3-inch HPSI substrates and SiC epitaxy with excellent intra-wafer sheet resistance uniformity (1.4%) has been demonstrated. SiC MESFETs fabricated on 2-inch wafers to baseline our manufacturing process prior to conversion to 3-inch demonstrated an average power density of 4 W/mm and very tight gate threshold voltage distributions. High temperature operating life (HTOL) testing of these devices has shown only a 2.5% reduction in drain current over the first 1,000 hours of operation. This is well below the JEDEC guideline of 20% for defining a failure and is indicative of a robust device and manufacturing process.

INTRODUCTION

Over the last several years, the development and demonstration of high power, high efficiency, and wide bandwidth amplifiers based on SiC MESFET devices has advanced rapidly [1]. By providing increased power density (~5X) and higher operating voltage, these devices will enable higher performance and lighter weight systems than those using conventional Si or GaAs technology. Using HPSI 4H-SiC substrates, the RF performance and reliability of SiC MESFETs has now matured sufficiently to be considered for a variety of military and commercial applications [2]. With the required device performance and operating life characteristics demonstrated in our 2" process, efforts have shifted toward bringing SiC MESFET costs in line with other traditional device technologies. This cost reduction will primarily be realized via a transition to 3-inch SiC substrates and epi, as well as, further improvements in device manufacturability. In this paper, we review the current quality of 3-inch HPSI SiC substrates and epitaxy. We then review current SiC MESFET performance and progress in the transition to 3-inch production capability.

HPSI 4H-SiC SUBSTRATES

The quality of HPSI 4H-SiC substrates is improving rapidly as illustrated in Figure 1.

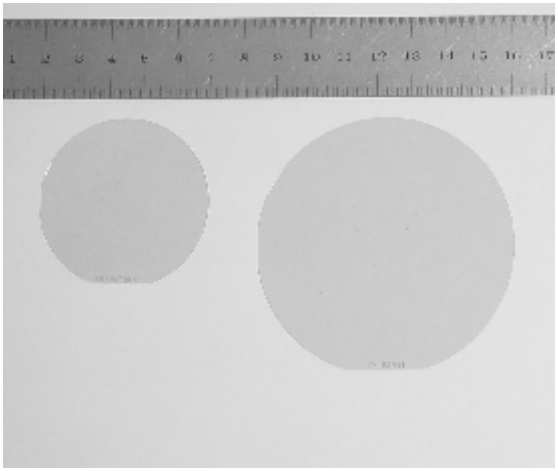

Figure 1. 2-inch and 3-inch HPSI SiC substrates

On the left side of Figure 1 is a production 2-inch 4H HPSI wafer and on the right side is a 3-inch 4H HPSI substrate. The quality of the 3-inch 4H HPSI substrates has improved to the point where "prototype" grade are now commercially available from Cree for advanced development use.

HPSI SUBSTRATE CRYSTAL QUALITY

Significant progress has been made in the reduction of all major crystal defects occurring in SiC bulk growth, most notably micropipes. The first major obstacle encountered when producing low micropipe 3-inch HPSI wafers was the lack of a viable micropipe counting method. The conventional etch process used for n-type wafers is chemically ineffective for HPSI substrates due to their non-reactivity. To circumvent this, an automated micropipe counting tool in conjunction with custom software is being developed. Figure 2 is a map of a 2-inch HPSI wafer that was generated using an early version of this tool.

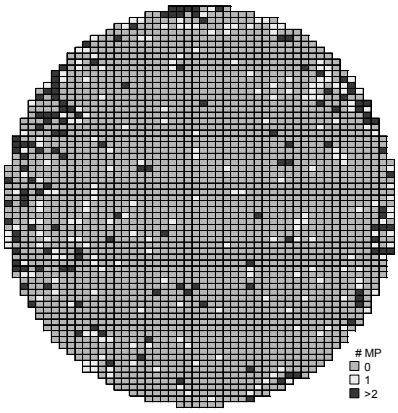

Figure 2. Micropipe map of a 2-inch HPSI substrate generated using our new automated micropipe counting tool. Each sampled area is 1.25 mm on a side. The key shows the number of micropipes counted in each sampled area.

To acquire the map shown in Figure 2, a wafer is loaded onto a stage. The automated tool then scans the wafer using optical transmission microscopy and visually identifies the number of micropipes in each field of view. The composite map is then recorded to a file. Although preliminary and not available for commercial substrates, this method promises to provide a faster, more reliable means of assessing the micropipe quality of our HPSI substrates than the current manually counted technique.

Figure 3 contains an "R&D best" wafer map for 3-inch HPSI substrates. The micropipe density of the 3-inch substrates is a very low 5 cm^{-2}. Not only has significant progress been made in reducing micropipe densities, but also current wafers exhibit very uniform stress profiles as shown in the stress birefringence images taken on low micropipe 3-inch wafers (Figure 4).

Typical 3-inch HPSI substrates are currently demonstrating an average micropipe density of 35 cm^{-2}. At this level, the yield loss due to micropipe defects is insignificant for most device peripheries.

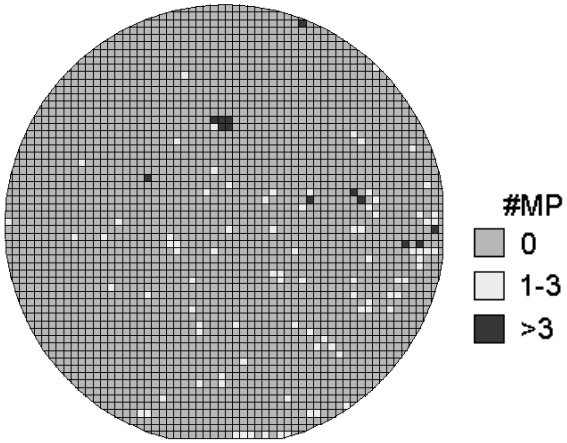

Figure 3. 3-inch micropipe map showing a micropipe density of only 5 cm^{-2}. Each sampled area is 1.25 mm on a side.

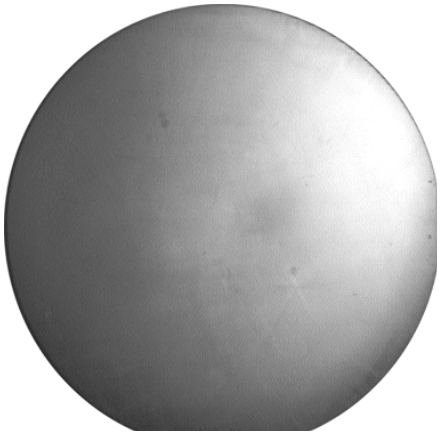

Figure 4. Cross-polarizer image of a 3-inch HPSI wafer exhibiting very low levels of contrast.

SiC EPITAXIAL DEVELOPMENT

Over the last six months, considerable progress has been made in the development of a 3-inch SiC epitaxy system suitable for use in the fabrication of high power SiC MESFETs. Figure 5 shows a schematic of the growth system used for this development. Process gases enter the system on the left side and exit on the right. During passage through the growth cell, some portion of the process gases react to form epilayers on wafers that rest on the platter.

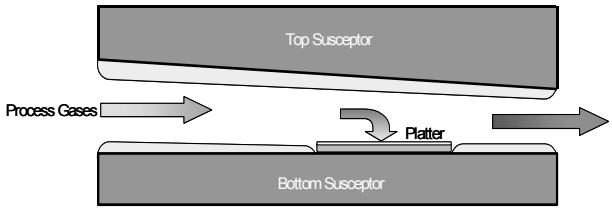

Figure 5. Schematic of our epilayer growth system

Figure 6 shows the resulting TLM derived sheet resistivity map for a 3-inch HPSI wafer using this system. As seen, an excellent 1.4% on-wafer variation has been demonstrated. Also note that 100% of the wafer has a resistivity within 5% of the wafer average. This is significant because our SiC MESFET production experience has demonstrated that all parts of a wafer that are within 5% of the average resistivity will pass our MESFET threshold voltage requirement. As a result, epilayer variation would not significantly contribute to device yield loss on this wafer.

SiC MESFET DEVICE FABRICATION

Using HPSI SiC substrates, the RF performance of SiC MESFETs is now sufficient to satisfy a variety of military and commercial applications. Figure 7 shows that over 5

W/mm and 60% power added efficiency has been demonstrated. Power output of 3.5 W/mm is now routinely produced from our baseline 2-inch process.

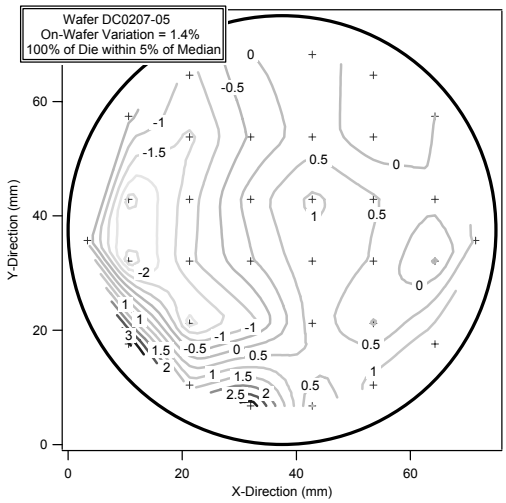

Figure 6. TLM derived sheet resistivity map showing excellent epi uniformity (1.4%) across a 3-inch HPSI wafer. Contours indicate difference from epi-wafer average.

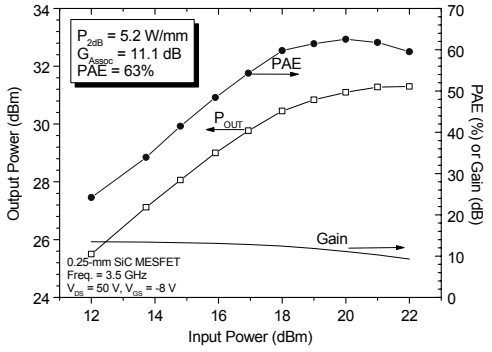

Figure 7. Output power and efficiency vs. input power at 3.5 GHz for a SiC MESFET fabricated on 4H HPSI SiC substrates

Prior to our SiC device fabrication facility converting to 3-inch capability, SiC MESFET device wafers were processed on 2-inch 4H HPSI wafers using the 3-inch epi reactor capability just discussed. To validate the quality of the epi produced in the 3-inch reactor, spacer rings were placed in the 3-inch system to allow growth on the 2-inch substrates. A device reticle was produced capable of stepping (1,035) 6-mm SiC FETs, along with ancillary test structures, across a 2-inch wafer as shown in Figure 8. Gate threshold voltage histogram plots are shown in Figure 9 for devices fabricated from these wafers versus the old epi system. The target gate threshold voltage for an optimum combination of channel current and breakdown voltage is –10 V. As seen in the Figure 9, the spread in threshold has improved considerably with the new epi. The tail out to –14 V in Figure 9 b) is due to thickness variation in the epi around the edge of the wafer.

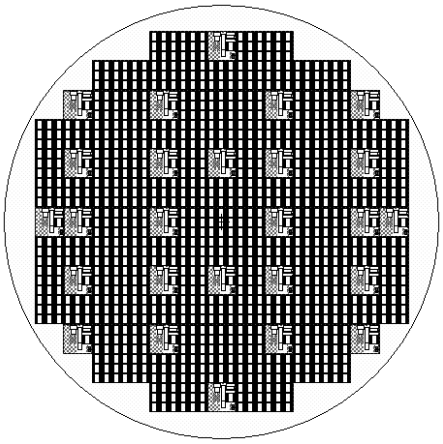

Figure 8. 2-inch wafer map with a total of (1,035) 6-mm SiC MESFETs and ancillary test structures

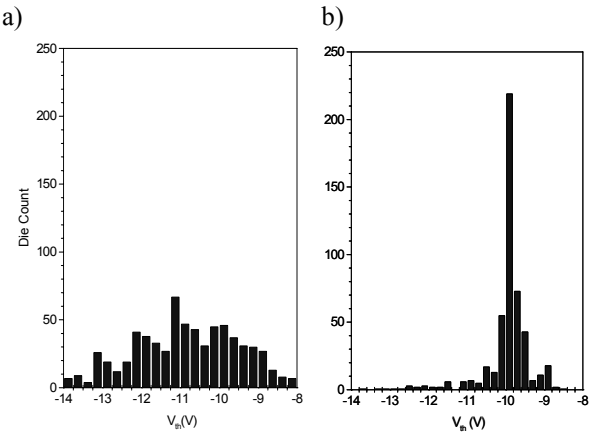

Figure 9. Histogram of V_{th} across a 2 inch SiC MESFET wafer for a) the baseline two-inch epi and b) the improved epi from the 3-inch system

On-wafer load pull measurements at 3.5 GHz under short pulse conditions were also performed on 6-mm FETs from each two-inch wafer processed using epi from the new reactor. As shown in Table 1, the average power density of the process is tightly controlled and averages 4 W/mm.

TABLE 1
Average of P_{3dB} measured with on wafer load pull at 3.5 GHz with a bias of V_{DS} = 50 V, I_{DS} = 150 mA.

Wafer	P_{3dB} (Watts)
1	4.29
2	3.89
3	3.63
4	4.03
5	4.04
6	4.04

Small signal measurements from a similar 6-wafer lot were taken on all DC-good FETs. From this data, small signal S-parameters were extracted (Table 2). This data demonstrates that not only are cross-wafer variations extremely small, but the distribution from wafer to wafer is also very tight indicating a well controlled process.

TABLE 2
Small signal parameters for 6-mm FETs across a 6-wafer device lot

	C_{GS}		C_{GD}		g_m	
Wafer	**Avg. (pF)**	**σ (%)**	**Avg. (fF)**	**σ (%)**	**Avg. (mS)**	**σ (%)**
1	2.83	1.8	496	1.9	127	1.5
2	2.82	1.0	454	1.3	125	1.5
3	2.82	2.1	509	1.8	127	1.8
4	2.93	1.8	477	1.7	132	1.4
5	2.94	1.9	520	2.2	134	1.7
6	2.91	1.3	477	2.0	129	1.6

SiC MESFET RELIABILITY

Forty-two MESFETs were packaged and DC high temperature operating life (HTOL) testing was performed for 1,000 hours on FETs from multiple wafers. The devices were biased to dissipate 4 W/mm and held at a constant gate voltage. The drain current was measured in-situ at temperature every 12 minutes. Figure 10 is a plot of the in-situ I_{DS} data for all 42 FETs. The average reduction in I_{DS} under these conditions was only 2.5%. Equally important is that there were no early failures and no out-of family behavior observed, indicating a well-controlled process.

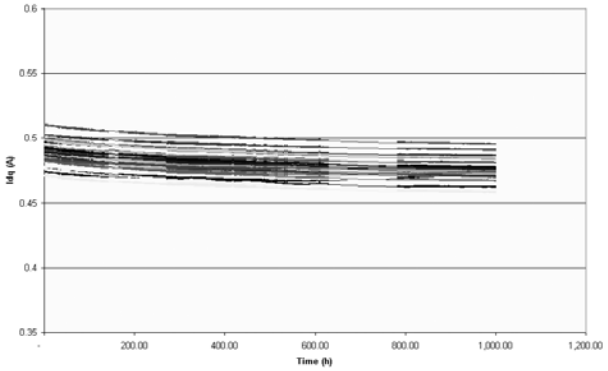

Figure 10. In-situ I_{DS} data for the 42 6-mm SiC MESFETs during HTOL testing at: V_{DS} = 50 V, I_{DS} = 500 mA (4 W/mm dissipated power), $T_{baseplate}$ = 90°C, $T_{junction}$ = 175°C

CONCLUSIONS

High quality 3-inch HPSI SiC substrates and associated SiC epitaxy have been developed to support the transition of SiC MESFETs to 3-inch production capability. Recent improvements in device processing have also been shown to support excellent device output power and efficiency, as well as high temperature operating life characteristics. The quality of our 3-inch substrates and epitaxy along with the repeatability of our 2-inch process gives us confidence in our transition to 3-inch fabrication. The first full 3-inch device lots are expected to be complete in early 2003.

ACKNOWLEDGEMENTS

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ACRONYMS

SiC: Silicon Carbide
HPSI: High Purity Semi-insulating
HTOL: High Temperature Operating Life
MESFET: Metal Semiconductor Field Effect Transistor

