Root Cause Analysis and Reduction of Off-State Leakage Current to Increase Manufacturability of a HIGFET Device

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Abstract

This paper will discuss the analysis and reduction of off-state leakage current on an enhancement mode hetero-structure insulated-gate FET device (EMODE). Due to the strict requirements for RF enabled devices, Off-state Drain to Source leakage (IDSOFF) was identified as a critical parameter during "the ramp phase" of this technology. This paper will address containment actions to minimize off-state leakage, key correlations of electrical parameters to off-state leakage, and characterization and experimental results of process modules affecting leakage.

I. INTRODUCTION

Developing a module for the wireless cell-phone market posed a unique and challenging set of requirements for Motorola. With more than 80 components in the module, the synergy between components is extremely important. The main constituents of the module, two EMODE devices used for high and low band signal amplification, directly influence the module performance.

During the ramp phase, it was determined that the off-state drain to source leakage distribution needed to be shifted in order to maximize yields. The leakage levels would need to be reduced by 80%. Figure 1 clearly shows that almost 75% of all electrical yield loss has been due to IDSOFF. This high yield loss represented the largest opportunity for yield improvement. The goal was to understand the components of IDSOFF and to enhance the process to increase the manufacturability of the technology.

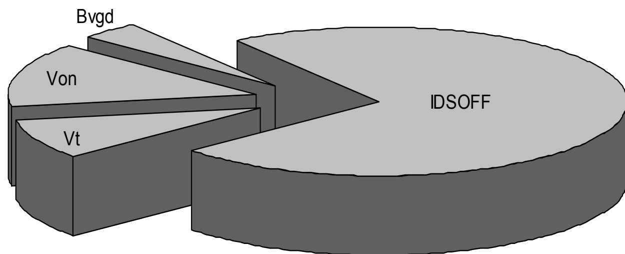

FIG. 1. Yield Loss Pareto

II. HISTORY

Historically, Process Control Modules (PCM) have been used to monitor and predict the performance of the actual device. Based on PCM to Unit Probe die yield correlations, the upper spec limit for IDSOFF at PCM was reduced from $5e^{-4}$mA/mm down to $1e^{-4}$mA/mm. The historical PCM histogram for IDSOFF appears in Figure 2.

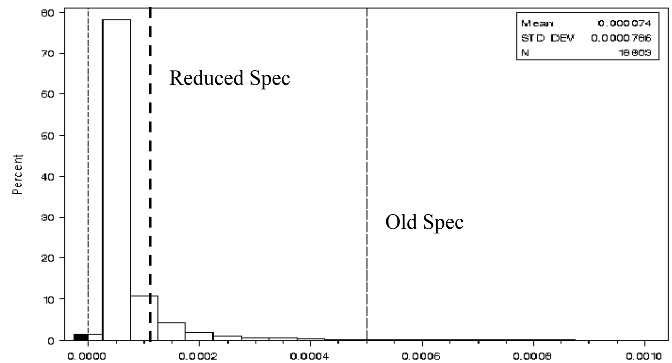

FIG. 2. IDSOFF PCM Histogram

Approximately 15% of tested sites failed the upper limit of $1e^{-4}$mA/mm. Investigation into the correlation of other device parameters to IDSOFF was completed. Correlations of Threshold Voltage (Vt) to IDSOFF indicated that a more positive Vt could help reduce the amount of drain to source leakage (Figure 3). In addition, increasing the gate length could be used to achieve additional process margin (Figure 4).

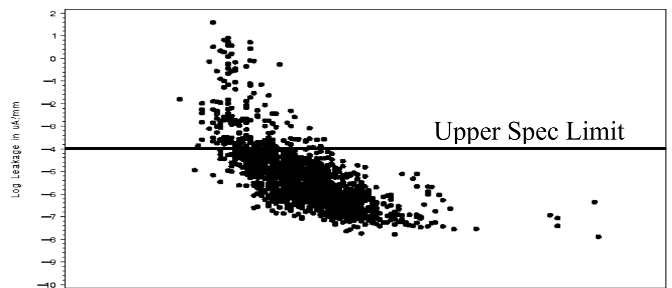

FIG. 3. Log IDSOFF vs Threshold

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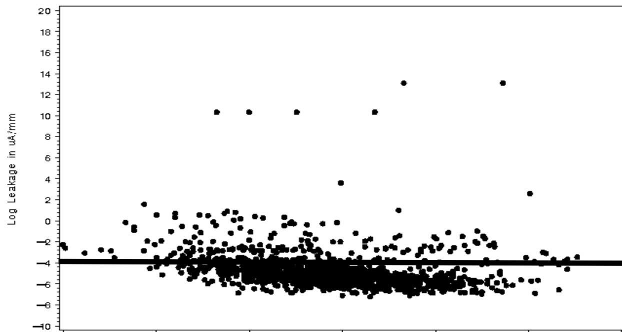

FIG. 4. Log IDSOFF vs Gate Length

Initial containment actions included increasing the threshold voltage and increasing the gate length to gain additional process margin for IDSOFF. As a result of this, the process windows for Vt and gate length were reduced.

III. ENHANCEMENTS TO PROCESS TECHNOLOGY

While the initial focus was on adjusting related PCM parameters to reduce IDSOFF, the tradeoff was that power output of the module was reduced. Additional process changes were required to reduce IDSOFF without impacting the RF performance of the device. The focus was directed to four key process areas: Rapid Thermal Anneal (RTA), Isolation Implant, the Gate Module, and Substrate/Epitaxial layers.

A. RTA

The first major improvement in leakage reduction was found at the isolation anneal module. During process development a 5sec RTA anneal was used. Split lots were run to investigate the impact of a 60sec RTA anneal. Results indicated that a 45% reduction in IDSOFF could be achieved by converting to the 60sec anneal (Figure 5). Theoretically the higher anneal time helped to repair any damage that was caused by the isolation implant.

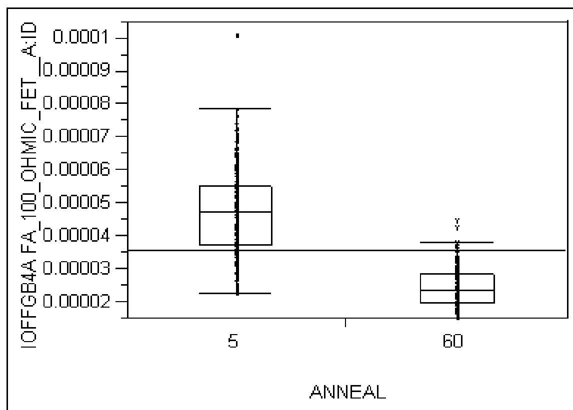

FIG. 5. IDSOFF vs RTA Anneal Time

B. ISOLATION IMPLANT

Given the results of the increase in RTA time for the isolation module, further optimization of the isolation implant was investigated. The current isolation implant scheme consists of a 90KeV followed by a 180KeV implant. SIMS analysis along with simulations (Figure 6) indicated that the 180KeV isolation implant might not be contacting the GaAs substrate, which may cause incomplete isolation of the devices. Split lots were run to investigate the impact of a 240KeV implant. Tests were done on known good material

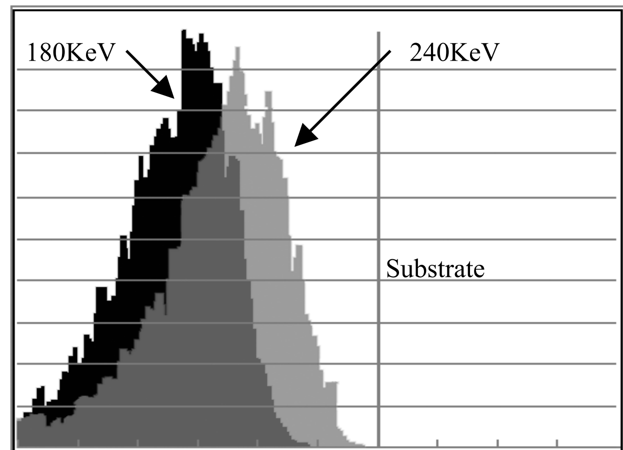

FIG. 6. Dose vs Implant Depth

and also on material known to have marginally high IDSOFF. Figure 7 shows that on marginal material a 60% reduction in IDSOFF was possible. On known good material, the higher energy implant had no effect on IDSOFF. All other device

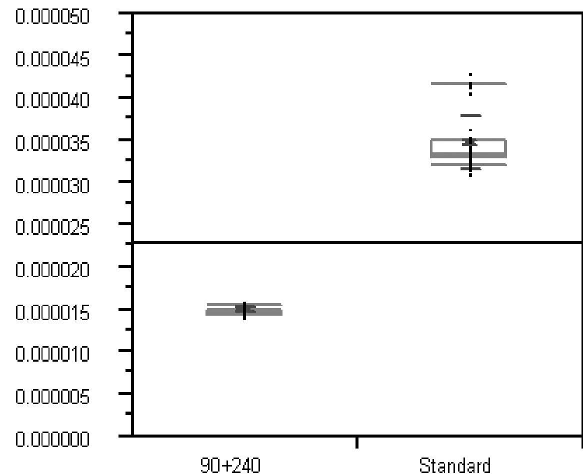

FIG. 7. IDSOFF vs Isolation Implant Energy

parameters were unaffected. By increasing the implant energy to 240KeV, material that was marginal for IDSOFF could now be used.

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C. GATE MODULE

As previously indicated, threshold voltage has a direct correlation to IDSOFF. In order to reduce leakage variation, threshold voltage needed to be tightly controlled. Threshold voltage is controlled by the properties of the epitaxial layers along with the gate metal deposition and gate length. To help control threshold voltage, the focus was put on gate metal deposition. During the metallization process, the deposition chamber is heated. As wafers are run through a deposition cycle, the system's shielding temperature increases due to heat transfer from the plasma. Preconditioning the deposition system prior to running production material was identified as a way to ensure that all wafers within a lot were exposed to consistent process conditions [1]. Figure 8 and 9 show that as a result of pre-conditioning, IDSOFF variation has been significantly reduced. Wafer to wafer variation of threshold voltage and gate metal sheet resistance has also been reduced with pre-conditioning.

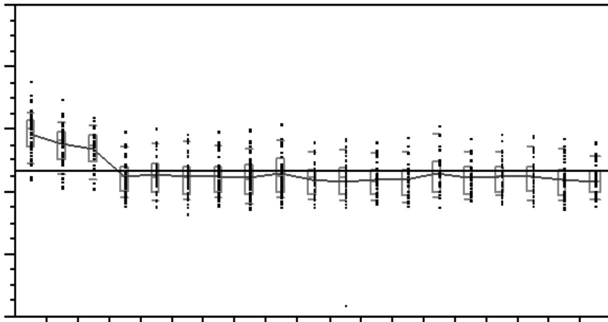

FIG. 8. IDSOFF vs Run Order w/o Pre-Conditioning

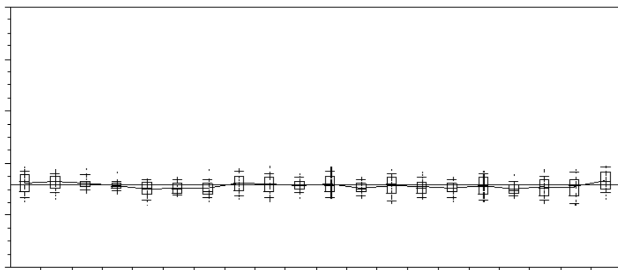

FIG. 9. IDSOFF vs Run Order with Pre-Conditioning

D. SUBSTRATE / EPITAXIAL

Further investigation into IDSOFF was focused on understanding the effect of the substrate and epitaxial layers. Figure 10 shows that substrate boule can have an affect on IDSOFF. Boules with higher IDSOFF were found to have a different processing characteristic that caused an increase in leakage. The solution was to apply spec limits to that characteristic, forcing a tighter distribution of incoming material.

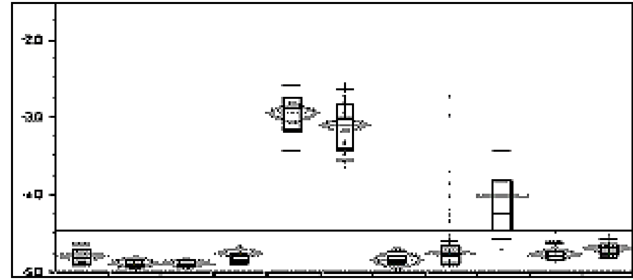

FIG. 10. Log IDSOFF vs Boule

In addition to substrate boule variation, we have found that differences exist between epitaxial vendors. Figure 11 shows that there is approximately an 8% difference in yield when comparing vendors. The main failure mode associated with the yield loss is IDSOFF. Split lots have confirmed that this difference is vendor related and not related to lot-to-lot variation. Based on experimental results and previous investigations [2], we suspect that most of the differences in IDSOFF can be attributed to slight differences in the buffer layer of the epitaxy. Although initial work has been done to understand these differences, additional work is necessary to fully understand the specifics surrounding the yield changes.

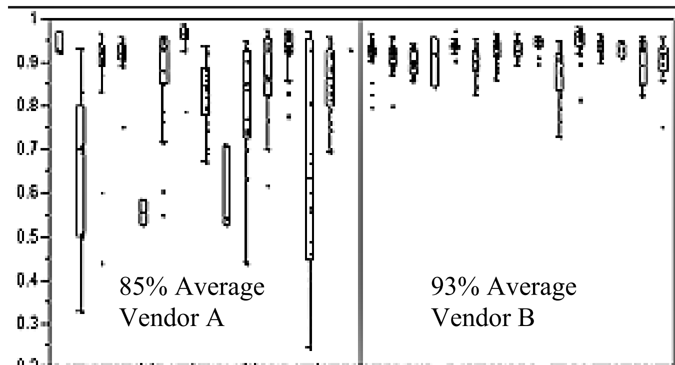

FIG. 11. Yield difference between Epitaxial vendors by Lot

IV. CONCLUSION

In an effort to understand the sources of off state drain to source leakage on EMODE devices we have performed extensive process splits and optimization experiments. Several areas were identified as possible contributors to yield loss associated with IDSOFF. As a result of the many experiments run, we now have a better understanding of the process and the technology. The primary improvements and findings include:

a) Increasing the isolation implant RTA time to 60 seconds reduced IDSOFF by 45%.
b) Increasing the Isolation implant to 240KeV can reduce IDSOFF by 60% on marginal material.

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c) Preconditioning the gate metal deposition system results in an increase in the uniformity of IDSOFF from wafer to wafer.
d) The realization that IDSOFF is dependent on boule and epitaxial vendor.

These changes and understandings have resulted in significant improvements in lot to lot control of IDSOFF. As a result, we have reduced our whole wafer scrap percentage for IDSOFF (Figure 12) and have consistently maintained high yields.

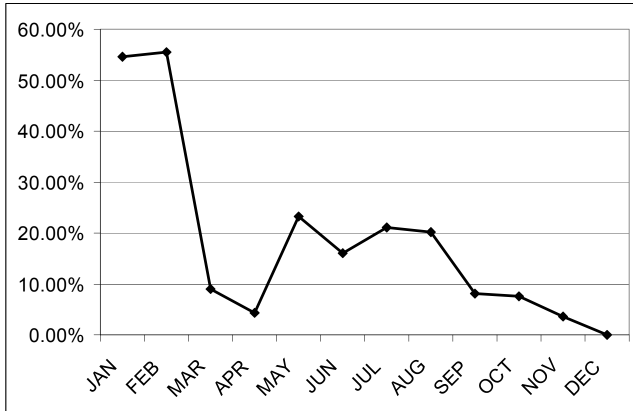

FIG. 12. IDSOFF whole wafer scrap as % of total scrap for technology

ACKNOWLEDGEMENTS

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ACRONYMS

HIGFET: hetero-structure Insulated-Gate FET device
EMODE: Enhancement Mode HIGFET
PCM: Process Control Module
IDSOFF: Off-State Drain to Source Leakage
Vt: Threshold Voltage
RTA: Rapid Thermal Anneal
SIMS: Secondary Ion Mass Spectroscopy