MIM's the Word – Capacitors for Fun and Profit

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Abstract

Capacitor properties were studied using a special test mask. We derived improved measurement and test capacitor and cell design. We saw a small perimeter scaling as well as the usual area scaling. Time dependent dielectric breakdown was extensively studied. We determined that the 4V/sec breakdown voltage is a sound figure of merit for that, and that nitride deposition conditions can be tuned for better TDDB performance, important for medium voltage applications. Capacitor nitrides as thin as 25 nm were seen to be feasible.

1. Introduction

Love me or love me not, I like the cap;
And it I will have, or I will have none.
Shakespeare, The Taming of the Shrew, Act iv. Sc. 3.

Bonny Kate was discussing a different kind of cap than we are accustomed to working with, but we like to have our caps, too. And more so than ever, they need to be better in all ways. This paper reviews work done to improve our Metal-Insulator-Metal (MIM) capacitors and our understanding of them.

TriQuint has featured metal-insulator-metal capacitors with 50 nm thick PECVD silicon nitride dielectrics for over ten years. The current process features sputtered metal for bottom and top plates. The bottom plate is our Metal 0, the first layer of local interconnect. The top MIM metal is itself not an interconnect metal, but is contacted by Metal 1, the first layer of global interconnect, through a via in the first inter-layer dielectric. In our layout rules, MIM metal is always included 2 um inside Metal 0, and Via 1 is always included 1 um within MIM metal.

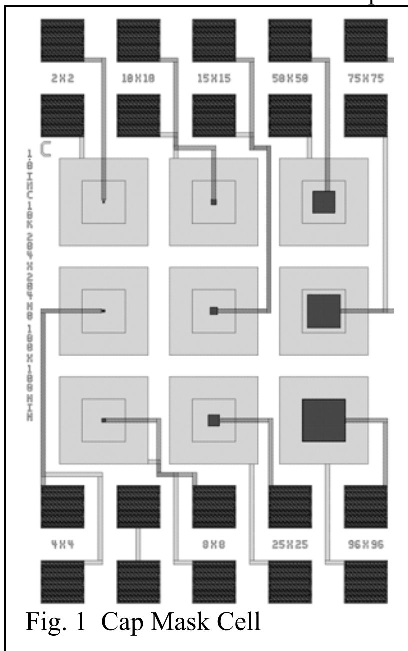


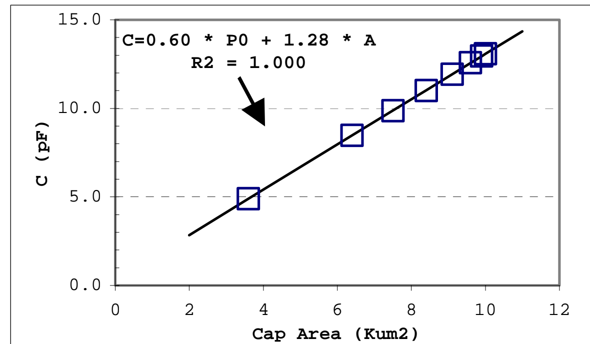
Fig. 1 Cap Mask Cell

The vehicles for this work were special capacitor test cells, such as shown in Fig. 1. The cell shown has 9 capacitors and uses two sets of our standard 2x5 probe pad arrays. Cell "C" is shown, which had 100 x 100 um MIM on 204 x 204 um Metal 0, with varying Via1 sizes. A whole mask was laid out with many variants of capacitor cells like this one, changing cap layout and shape, Via1 location and dimension, bottom plate contact scheme, etc. This mask was used in short loop runs with only capacitor and interconnect fab steps. In addition, some cells were placed in our foundry full flow "pizza" masks to investigate the effects of a full MESFET process flow on capacitor properties. We focused on our normal 50 nm nitride caps, but also examined thicker and thinner nitride dielectrics, going as thin as a nominal 25 nm.

2. Metrology and Test Capacitor Design

Our usual practice was to measure process control module test capacitors by contacting the capacitor briefly, then breaking contact to measure stray capacitance for cancellation. To investigate that, duplicate cells were made for all variants that were exactly identical to the cells save for having no via connecting the top metal line to the capacitor top plate. Measuring this structure provides essentially perfect stray C cancellation. It was found that the difference between this method and the standard method increased for middle capacitors in the array, and increased with via size (and accompanying Metal 1 size). However, in the worst case it was only a few tenths of pF, and so of little consequence for test capacitances of tens of pF such as we use. However, this suggests great care must be taken for testing low value capacitors, and that a good standard test cap should have a value of a few tens of pF for a robust test.

One layout variation included sharing one large bottom plate for multiple top plates. This led to a shift in all measured capacitances. However, no shift was seen when separate bottom plates were all connected individually to a shared common bond pad, allowing 9 test caps in a single 2x5 array.



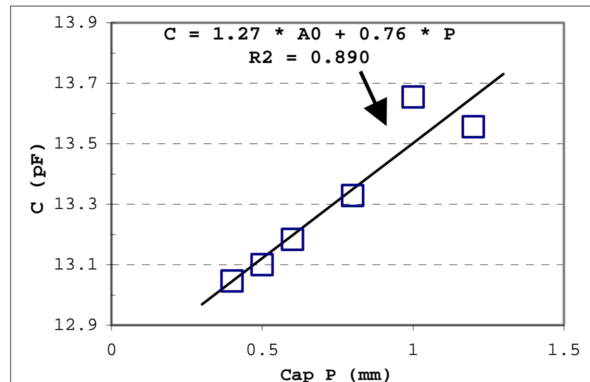


Fig. 2 Capacitor Scaling

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3. Scaling

The usual assumption is that MIM capacitance scales with MIM metal area. The test mask included one cell with varying areas for a constant 400 um perimeter and another cell with a constant 10 Kum^2 area and varying perimeters. Examples of test results for those cells in one site (50 nm nitride thickness) are shown in Fig. 2. The top graph shows capacitance vs. area (constant perimeter), the bottom capacitance vs. perimeter (constant area). In a typical case, fitting (site by site for 109 sites of each cell) to a model assumed linear in both area and perimeter, we get

$$C\ (fF) = (1.25 \pm 0.02) * A\ (um^2) + (0.60 \pm 0.04) * P\ (um),$$

where the factors are (average ± one standard deviation).

We see that capacitance does depend slightly on perimeter, if not accurately linearly (Fig. 2). In practice, the perimeter effect is much smaller than that of area and would usually be swamped by MIM nitride thickness variations, typically a few percent over a wafer. However, this result would be useful for matching closely spaced capacitor pairs as exactly as possible.

4. Time Dependent Dielectric Breakdown (TDDB)

MIM capacitor leakage slowly decreases with time until breaking down catastrophically, as shown for typical 50 nm capacitors with 30 Volts applied in Fig. 3. This TDDB has

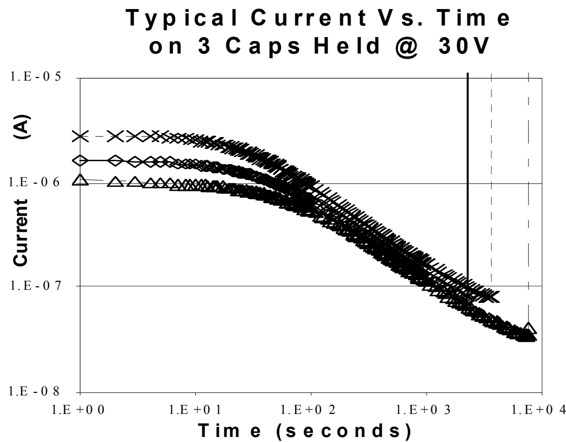


Fig. 3 TDDB Example

intrinsic (dielectric strength) and extrinsic (particle related) components and is well known in the literature [e.g.1-3]. The breakdown occurs at progressively shorter times as the applied voltage is increased.

In the standard "static" TDDB test, this time is measured for several voltages large enough to effect failure in short times, and a long extrapolation is made to a low voltage lifetime to give a common figure of merit for the capacitor. However, the data is invariably very noisy, and the extrapolation very long, giving huge errors in the TDDB lifetime, as illustrated in Fig. 4. That figure shows typical static TDDB results measured at 42, 44, 46, and 48 V for 50-140 sites from several runs. A weighted least squares line fit was done to derive average and deviations for slope and intercept, and "±1 standard deviation" lines are displayed, just to illustrate the tremendous noise in this figure of merit.

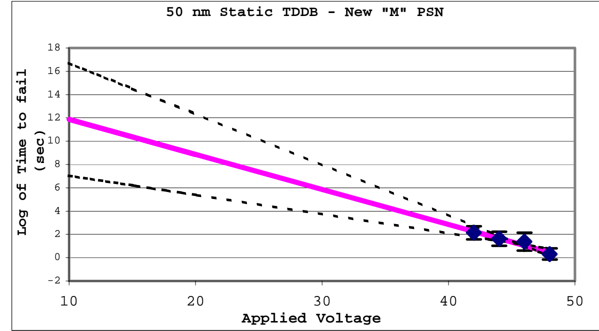


Fig. 4 Example of static TDDB test

Beall et al [4] of TriQuint/Texas discussed a simpler figure of merit for TDDB. The test simply applies a 4V/sec ramped voltage to the capacitor and records the voltage where breakdown is seen. We have concluded that the 4V/sec ramp breakdown voltage is well behaved, and represents the best figure of merit for capacitor TDDB. If static TDDB tests are done at all, the results are usually viewed as times to fail at the given voltage to avoid the possibly misleading lifetime at low voltage derived solely from high voltage measurements.

Our 50 nm capacitor has proven robust enough for most wireless and digital low voltage applications, but several recent medium voltage applications have required us to work towards a higher dielectric strength (higher TDDB lifetime or 4V/sec breakdown voltage). As shown below, TDDB is very sensitive to MIM nitride thickness, but that approach is undesirable.

TDDB was seen to not be influenced by Metal 0 stress or

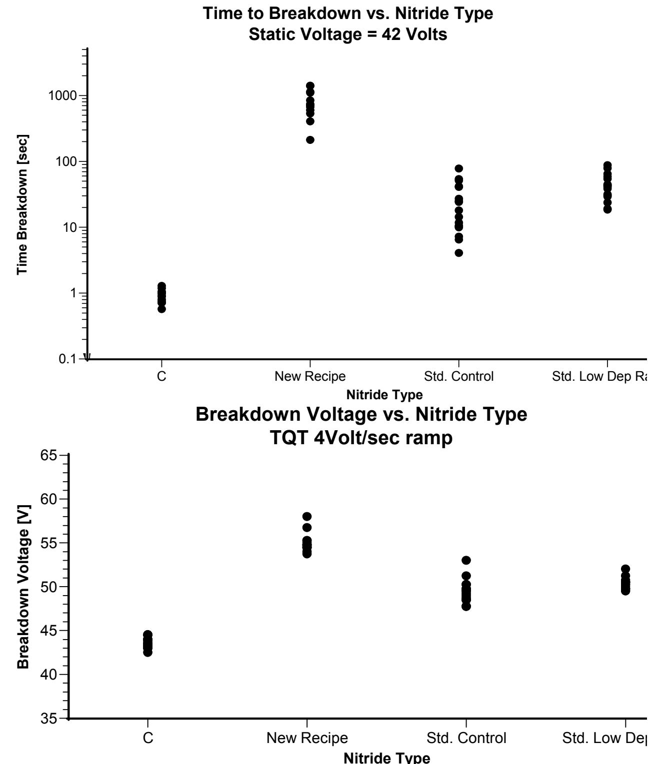


Fig. 5 Two TDDB Representations of a New Nitride

pre-deposition treatment (which affects surface roughness). Nitride deposition conditions were next investigated, and we found a recipe that gives much better TDDB performance, as shown in Fig. 5, as well as one much worse ("C").

This new nitride has similar physical characteristics to our old nitride, but the new nitride gives substantially lower capacitor leakage current and much better TDDB performance for the same dielectric thickness (Fig. 5).

The enhanced new nitride led us to investigate the feasibility of making capacitors with even thinner dielectrics. Nitride thicknesses of 25, 35, and 45 nm were fabricated on a full flow "pizza mask" run to include all effects that would occur in normal production use. Good uniformity and capacitance per unit area were obtained, as shown in Fig. 6. The figure shows MIM parameters for the experimental nitride thicknesses of 25, 35, 45, and 50 nm and demonstrates that thinner nitrides can be reasonably uniformly deposited.

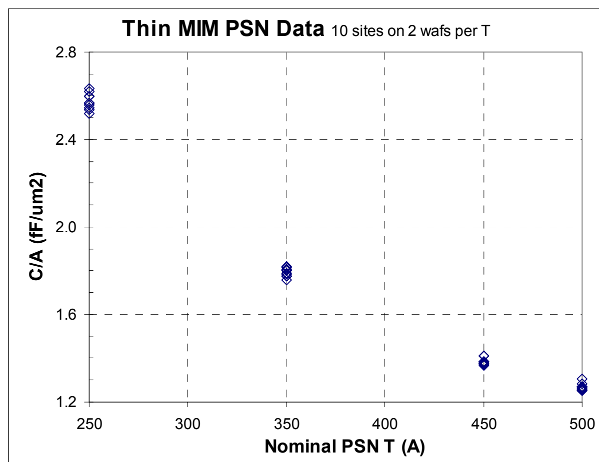


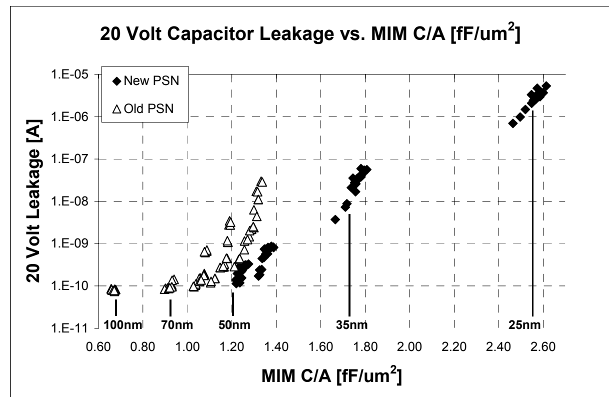
Fig. 6 Nitride Thickness Experiment Results

One non-destructive indicator of TDDB performance is the capacitor leakage current with 20 V applied, a standard capacitor measurement at TriQuint. Our tests have shown that for nitrides thicker than 50 nm, MIM cap leakage currents at lower voltages can often just be measuring the leakage between the test pads.

Capacitor leakage and 4 V/sec ramp breakdown voltage data for the old and new nitrides over thickness are shown in Fig. 7. We have seen that 50 nm of the new nitride has a TDDB performance about the same as 60 nm of the old, a very substantial improvement. Moreover, this stronger nitride makes the practical use of even thinner nitrides conceivable for higher capacitance per unit area without excessive leakage. While 25 nm capacitors may not currently be practical, this data suggests one can go well below 50 nm for many applications. Work in this area continues at TriQuint.

5. Conclusions

We have reviewed some results of recent studies of MIM capacitors. A better understanding of our capacitors and how to test them has resulted, and we have been able to improve their performance in a number of areas. Some of these are directly transferable to other fabs and processes, but the others at least suggest avenues to pursue for improvement with each fab's specific tool set.



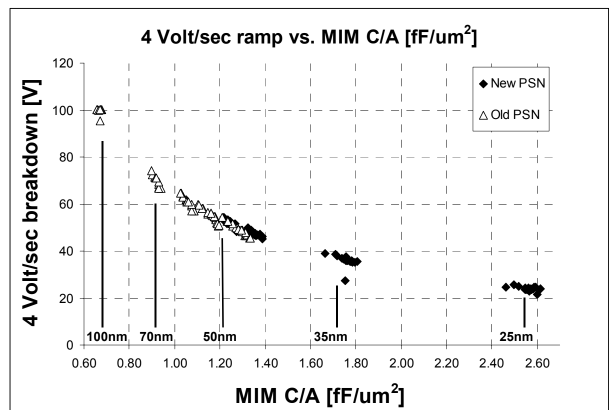


Fig. 7 Composite TDDB Results, New and Old Nitride

6. Acknowledgments

We would like to thank our colleagues in process engineering and production at TriQuint Oregon for their consistent help and support, and the authors of reference [4] and other TriQuint Texas colleagues for valuable discussions and suggestions.

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Acronyms

PECVD: Plasma Enhanced Chemical Vapor Dep.
MESFET: MEtal Semicond. Field Effect Transistor
MIM cap: Metal Insulator Metal capacitor
TDDB: Time Dependent Dielectric Breakdown
PSN: Plasma Silicon Nitride
TQT: TriQuint Texas

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