Wafer-Level Assembly of Heterogeneous Technologies

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Abstract

A technology platform demonstrating wafer-level assembly of heterogeneous technologies based upon vertical wafer stacking is described. This platform offers the potential for low-cost assembly of various compound semiconductor circuits with silicon ICs for wide bandwidth optoelectronic and space-conservative packaging applications. Process development results obtained to date are presented, and approaches to heterogeneous integration using this novel technology platform are outlined.

INTRODUCTION

Wafer-level assembly of heterogeneous technologies based on wafer-level three-dimensional integrated circuits (3D-ICs) offers the opportunity of reduced manufacturing cost for highly integrated systems, while providing high performance interconnects and high packing density [1-6]. In the past few years, various approaches have been aggressively pursued for wafer-level 3D-ICs [2-11]. Initial focus has been on microprocessors, application specific ICs (ASICs) and memories, but extensions to heterogeneous integration (also referred to as hyper-integration) including RF, analog, optical, and micro-electro-mechanical systems (MEMS) are also being explored [1-6].

Process technologies to achieve 3D ICs include embedded thin film transistors (TFTs) [7] or wafer bonding using vias to internally connect the stacked wafers. Wafer bonding technology using metal as a bonding agent [8-10] or using dielectric adhesive glues [3,4,10,11] are being developed, compatible with micron-sized vias for inter-wafer interconnection. While having electronic interconnect advantages to meet semiconductor roadmap limitations [2], they differ in processing requirements and extendibility to non-electronic heterogeneous integration.

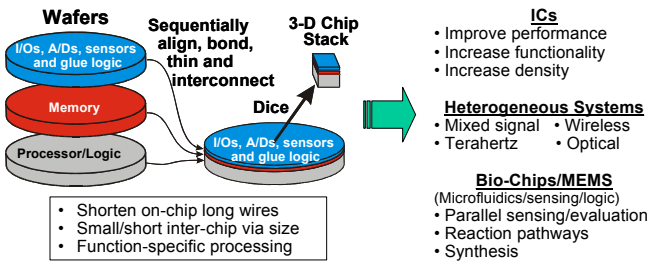

Fig. 1. Hyper-integration platform based on 3D vertical integration for future IC chips and heterogeneous systems, formed by monolithic wafer alignment, bonding, thinning and inter-wafer interconnection.

In this paper, we present process development results with our approach to wafer-level 3D ICs and discuss its extensions to other heterogeneous technologies. Our hyper-integration approach is to bond dissimilar wafers with a dielectric glue after micron-scale alignment, followed by the top wafer thinning and inter-wafer interconnection. As depicted in Fig. 1, such a technology offers the promise of low-cost assembly of various compound semiconductor circuits with silicon ICs for broad bandwidth optoelectronic applications and space-conservative packaging needs.

ELECTRONIC HYPER-INTEGRATION TECHNOLOGY PLATFORM

Fig. 2 shows a test structure of a three-wafer stack for processing development of our electronic hyper-integration technology platform. The fully processed wafers (with multilevel interconnects) are aligned and bonded with a dielectric polymer glue, followed by top-wafer thinning to less than 10 μm using backside grinding, polishing and etching. Subsequently, inter-wafer interconnects are formed using a copper damascene process, including high-aspect-ratio (HAR) via etching, copper deposition and chemical-mechanical planarization (CMP). A viable baseline process flow to address the key challenges indicated in Fig. 2 has been established with 200 mm silicon wafers and thermal coefficient-of-expansion (TCE) matched glass substrates. Processing temperatures below 300 °C and bonding pressures below 50 psi have been used without damage with multilevel-metal Si test wafers. The experimental results to date along with baseline process flow are discussed in this section.

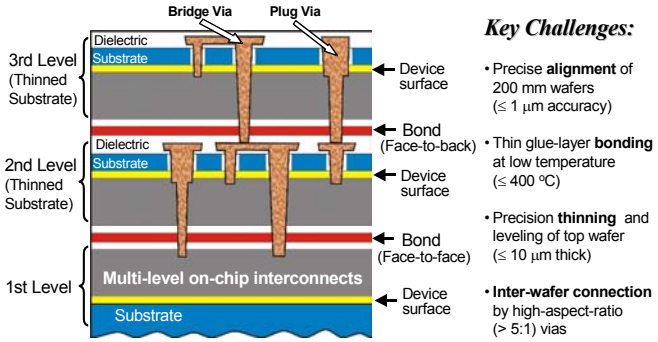

Fig. 2. Schematic of a hyper-integration 3D test vehicle using wafer bonding, showing bonding interface, vertical inter-wafer vias (plug- and bridge-type), and "face-to-face" and "face-to-back" bonding.

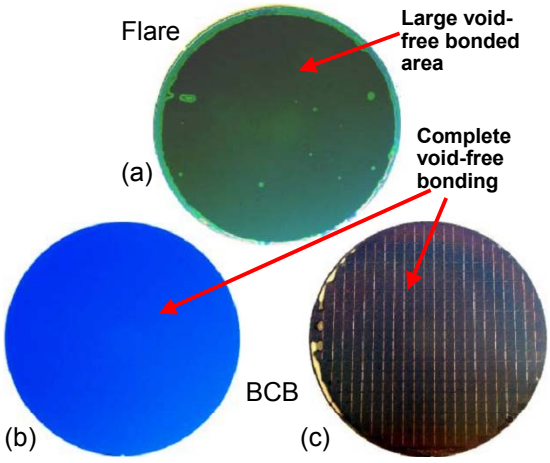

Fig. 3. Wafer bonding results [3]: (a) Corning glass 7740 bonded to Prime Si with Flare, (b) PG&O glass 1737 bonded to Prime Si with BCB, and (c) two via-chain patterned wafers bonded with BCB. No visible changes can be observed after Si wafers are thinned to ~ 30 µm.

Wafer Bonding and Thinning

Wafer-to-wafer bonding has been studied using various dielectric glues with both blanket wafers and processed wafers. The wafer bonding is conducted in a vacuum chamber of an EV Group (EVG) 501 bonder at conditions (e.g., temperature) compatible with silicon back-end-of-the-line (BEOL) processes. Fig. 3a shows wafer bonding result using Flare (Poly aryl ether) as the bonding glue on blanket wafers, while Figs. 3b and 3c show wafer bonding results using benzocyclobutene (BCB) as the bonding glue on blanket wafers and our via-chain patterned wafers, respectively. In Figs. 3a and 3b, a silicon wafer is bonded to a commercial TCE-matched glass wafer so that bonding uniformity can be visually inspected through the glass wafer. Void-free bonding is obtained with BCB and high bonding strength is achieved with both BCB and Flare.

Subsequent to wafer bonding, the top Si wafer is thinned to less than 10 µm and leveled to minimize the inter-chip via length and aspect ratio. A two-step thinning process is established to minimize mechanical damage. In the first step, the backside Si substrate is uniformly thinned to less than 50 µm by mechanical grinding and polishing (CMP). In our via-chain fabrication and wafer thinning with SOI wafers, the baseline second-step thinning process uses tetramethyl-ammonium hydroxide (TMAH) as the Si etchant due to its compatibility with CMOS process and excellent selectivity to SiO_2 (selectivity as high as 6000 has been obtained using this approach).

Fig. 4 shows a photo image of a 200 mm wafer with state-of-the-art copper interconnect structures, which is bonded to a TCE-matched glass wafer and thinned to 35 µm using our baseline bonding and first step thinning processes. Though the pre-bonded wafer surface profile shows a step height of ~ 0.9 µm across the Al pads (see in Fig. 4), void-free bonding and damage-free patterns are maintained after wafer thinning. Electrical tests on the interconnect wafer are

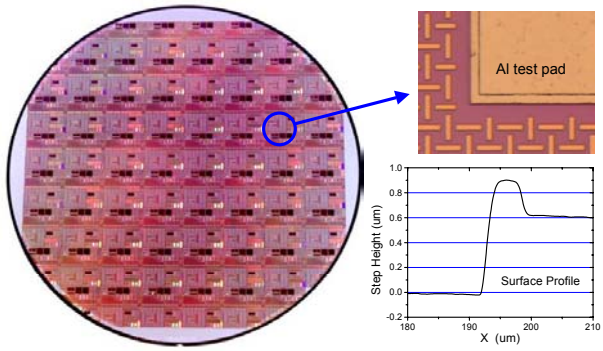

Fig. 4. Image of wafer with multi-level Cu-interconnects (provided by International SEMATECH) bonded on a glass wafer and backside thinned to 35 µm. Right side: surface profile showing a step height of ~ 0.9 µm across the Al pads.

performed after bonding, thinning, top silicon removal (wet-etch) and BCB ashing in order to re-expose bond pads for electrical testing, and comparison to original data. The changes in the via resistance and the comb-to-comb leakage current are within the acceptable limits [3].

Inter-Wafer Interconnects

In order to evaluate the processing feasibility and to establish design rules for the inter-wafer interconnect technology using dielectric wafer bonding, a four-layer mask set of via-chain test structures has been developed with features for testing both bridge and plug types of vias. Fig. 5 illustrates the inter-wafer interconnect process flow, showing plug- and bridge-type vias, including processes of wafer-to-wafer alignment, HAR via etching and cleaning, liner and copper filling, and CMP. The Si substrate on the top wafer is completely removed by backgrinding, polishing, and wet-etching in order to simplify and focus on the inter-wafer interconnect process. Except for wafer-to-wafer alignment and bonding, conventional Cu damascene BEOL processes are used for this test structure.

Images in Fig. 6 show plug- and bridge-type via-chain patterns for a two-micron via with different landing pads,

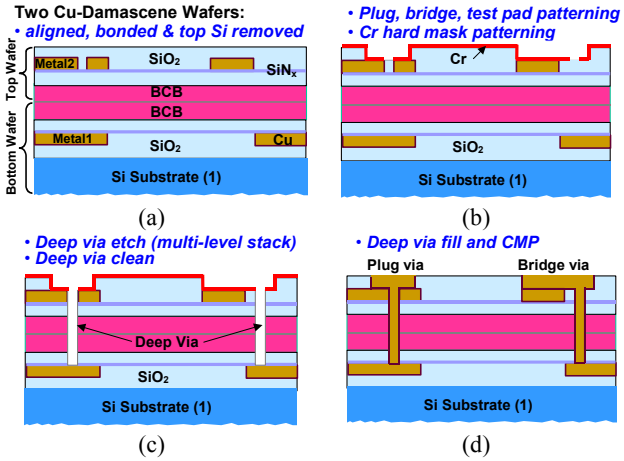

Fig. 5. Inter-wafer interconnect process flow for via-chain structure fabrication.

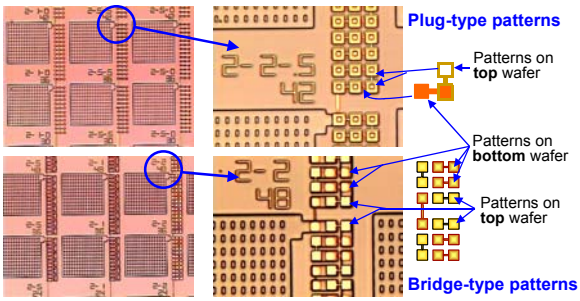

Fig. 6. 200 mm wafer-to-wafer alignment accuracy with via-chain test structures, indicating 1 µm alignment can be achieved (<0.5 µm shown).

plug sizes (for plug type) and chain lengths, prior to deep via processing. These photographs are taken on a pair of Cu-damascene wafers after alignment, bonding and top wafer thinning using our baseline process with the top Si substrate completely etched, and bridge lines, plug pads and test pads patterned. One-micron wafer-to-wafer alignment accuracy are achieved using an EVG wafer aligner with SmartView™ technology, though the alignment accuracy varies over the 200 mm wafer pair, which needs to be addressed together with, at least, wafer bow, lithography and wafer bonding.

The inter-wafer interconnect formation requires etching a via of the order of 10 µm deep, through a multi-level/material stack (such as SiO_2 or other low-k dielectric with etch-stop, silicon nitride, and bonding adhesive layer). Control of the sidewall profile with a variety of materials is challenging, and the etch rate may not be uniform due to via-size differences and etch-chamber loading effects. In this work, a 0.2 µm chromium layer is used as the hard mask for the deep via etching. A design-of-experiment procedure was used to study the deep via etch through various materials on either blanket films or multi-material structures, using a 200 mm wafer capable inductively coupled plasma (ICP) reactor. A HAR via etch processing is thus established [3].

Prior to via filling after etching, a two-step via cleaning is used, i.e., wet-chemical cleaning followed by plasma dry clean. For via filling, a low temperature (< 300°C) TaN liner process is carried out in a custom designed load-locked 200 mm wafer chemical vapor deposition (CVD) tool. The Cu CVD fill is performed on a modified Tokyo Electron (TEL) Phoenix 200 mm wafer cluster tool. A physical vapor deposition (PVD) copper flash layer is applied prior to CVD copper fill in order to enhance the adhesion of the thick stack. Finally, CMP of such structures to complete the copper damascene process has been demonstrated [3].

With the process development discussed above, we are able to fabricate the via-chain test structures; wafers are currently undergoing electrical testing. Detailed analysis of the electrical data and cross-section inspection of the via-chain structures will be used to improve the inter-wafer interconnect process and design the next generation via-chain structures.

Optical-Electronic Hyper-Integrations

Based on the processing technology developed with electronic hyper-integration, we propose three alternatives of optical-electronic hyper-integration to further enhance the interconnect performance, as shown in Fig. 7. The lower two levels in the stack are similar to that in Fig. 2, e.g., a high speed processor (bottom) and a memory (middle). However, the third wafer (top wafer) in Fig. 7a is an optical wafer, which has photo detectors within the opto-electronic circuitry and optical waveguides with optical mirrors. The optical signal coupled onto the chip from an off-chip source can be modulated and distributed through waveguides. It can then be focused vertically to the detector by an optical mirror [12], and converted to the electrical signal through a receiver circuitry. The electrical vias provide the inter-wafer interconnects and inputs/outputs (I/Os).

Fig. 7 also shows other alternatives. Here, optical signals after modulation and distribution through the waveguides are directly coupled down to the lower wafers either by optical waveguide vias (Fig. 7b) or optical beam vias (Fig. 7c). The waveguides and optical mirrors are formed directly on top of the stack. The opto-electronic circuitry with photo detectors is fabricated on the lower wafers with constraints in material and processing. An initial analysis using a FullWAVE simulator for these two types of via is shown in Fig. 8, i.e., the divergence of optical beam in a multilevel stack (830 nm beam with TE polarization and 2 µm core width). As shown

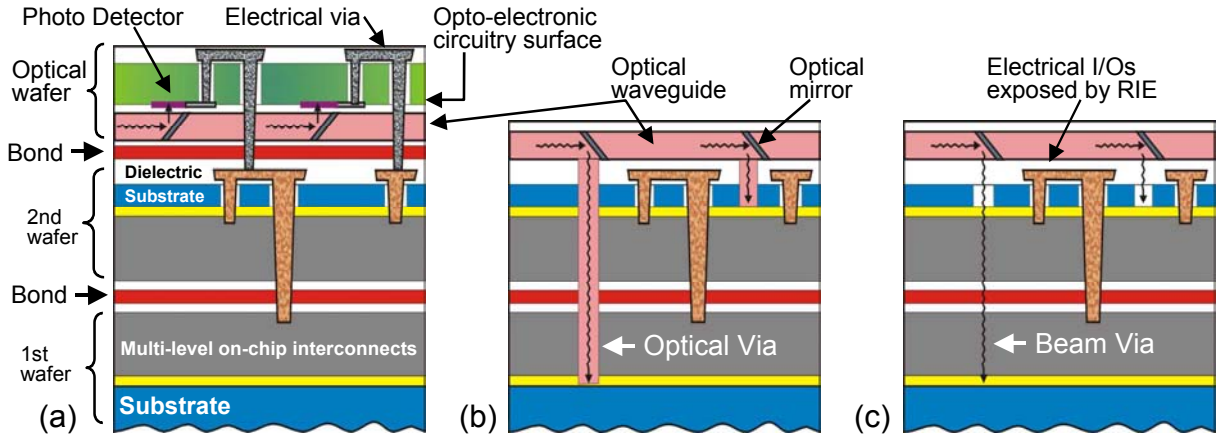

Fig. 7. Schematics of optical-electronic hyper-integration with (a) electrical vias, (b) optical waveguide vias and (c) optical beam vias.

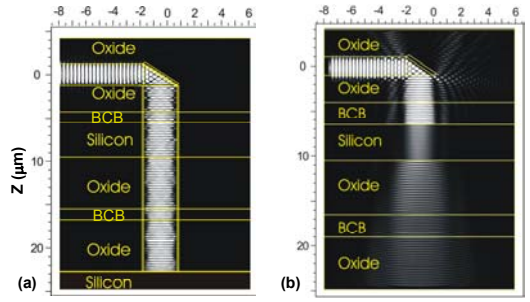

Fig. 8. Simulation result of the divergence of an optical beam through multilevel materials: (a) with an optical waveguide via filled by polymer with a refractive index of 1.51, and (b) without an optical via.

in Fig. 8a, a transmission as high as 96% can be obtained for the optical waveguide via. Some loss can be seen on Fig. 8b for the optical beam via; an anti-reflection coating and an partial optical via through the Si substrate may be used to minimize the losses through the multiple layer.

Similarly, the top wafer in Fig. 7a can be a GaAs (or other compound semiconductor) wafer with microwave or optical/photonic circuitry. While bonding of compound semiconductor wafer directly to silicon is realized, a high-power light emission diode (LED) is also made by bonding an AlGaInP LED epiwafer to a Si substrate, after which the light-absorbing GaAs substrate is removed [13]. However, with the hyper-integration technology discussed in this paper, the GaAs wafer and Si wafer can be processed separately with their own optimal processing conditions. They are then aligned and bonded using a dielectric glue, followed by inter-wafer interconnection to facilitate a GaAs-Si system integration. Unlike the directly bonded GaAs-on-Si approach, this hyper-integration approach allows integration of GaAs circuitry with a Si CMOS wafer without processing constraints, such as lattice mismatch, thermal budget during processing, and interconnect incompatibility. New generations of either GaAs or silicon design and processing technology can be implemented into existing GaAs-Si systems with minimum design/processing development efforts prior to manufacturing. However, common wafer diameters and dies sizes seem to be required.

PACKAGING

This monolithic hyper-integration also allows innovative packaging. As depicted in Fig. 9, a generic hyper-integration package assembly envisioned includes a high density of I/O contacts using flip-chip solder bumps or sea-of-leads contacts [14] to a thin film structure. In addition to the inter-wafer vias, large vias through the stack are used for heat sinking (cooling), electrical isolation and power distribution purposes. A flexible backplane can be included for additional I/O capability (e.g., optical, RF or power). With this approach, a package with very high density, high performance and high functionality can be achieved with a chip-stack only 20 to 30 µm thicker than a single die, without limiting the post-dicing packaging processing.

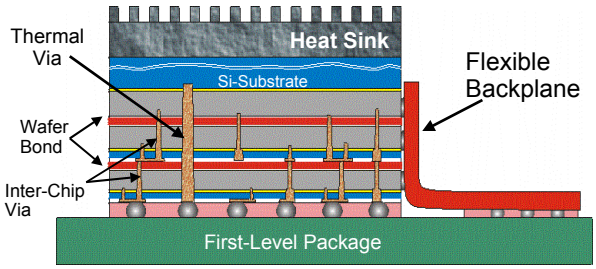

Fig. 9. Package assembly envisioned with hyper-integration technology. Thermal and ground vias enable cooling and electrical isolation; flexible backplane (edge contracts) offers additional I/O capability.

CONCLUSIONS

Electronic hyper-integration using our 3D IC technology platform can improve digital system performance by reducing global interconnect delays. Moreover, this generic platform enables wafer-level assembly of heterogeneous technologies such as GaAs or InP electronic or photonic circuits with Si ICs for high performance and low cost applications. Extensions to such photonic-electronic integration can be achieved with electrical, optical waveguide or optical beam vias, depending upon bandwidth needs and processing constraints. A packaging concept for such a 3D platform is compatible with current high-performance, space-conservative packaging approaches.

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