DENSE, TWO-DIMENSIONAL OPTOELECTRONIC CHIPS FOR HIGH-SPEED, PARALLEL OPTICAL LINKS

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Abstract

Two-dimensional opto-electronic chips are gaining acceptance as a means to dramatically increase data transfer bandwidths. Thermal issues combine with the laws of statistics to stand in the way of achieving the low failure rates demanded by system engineers. Redundancy constitutes a promising avenue to pursue for circumventing the problem and ensuring the desired component life expectancies.

INTRODUCTION

The expanding demand for higher data traffic rates is driving the industry toward gradually replacing the currently favored linear arrays (1x4 to 1x12) of optical transmitters (Tx) and receivers (Rx) with a new generation of two-dimensional arrays. For example, TeraConnect, Inc., currently offers a line of transmitter and receiver modules based on 24- (2x12) and 48-channel (4x12) optoelectronic (OE) chips suitable for short-reach applications up to 300 meters. These modules operate at a wavelength of 850 nm and at speeds up to 3.2 Gb/s per channel, supporting aggregate data rates in excess of 75 and 150 Gb/s, respectively. This paper describes the manufacture and performance of these modules and addresses some of the unique challenges presented by this emerging technology.

MODULE FABRICATION/PERFORMANCE

Our optical transmitters are based on two-dimensional arrays of GaAs/AlGaAs bottom-emitting VCSELs designed to emit at 850 nm. Likewise, detector arrays consist of GaAs/AlGaAs p-i-n photodiodes, all on a 125-μm 2D pitch. Wafers go through a sequence of front-side processing steps which result in a 2D array of electrically isolated emitters/detectors with two contacting pads per unit cell, as shown in Figure 1. The arrays are flip-chip bonded to custom-designed, matching SiGe ASICs incorporating laser diode drivers in the case of VCSELs and transimpedance amplifiers/ comparators in the case of PIN diodes. In both cases, an epoxy underfill is wicked between the active chip and its corresponding ASIC to enhance the mechanical integrity of the composite structure. This step enables the total removal (via mechanical/chemical means) of the substrate following hybridization, allowing the light to exit from or impinge onto the relevant

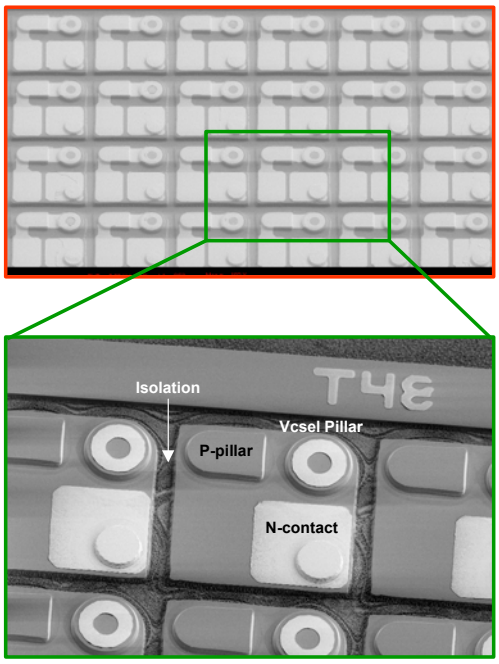

Fig. 1: SEM photos of portion of a 4x12 VCSEL array prior to bump deposition and hybridization. Unit cells are electrically isolated from each other and feature two electrical contact pads. The pitch is 125 μm.

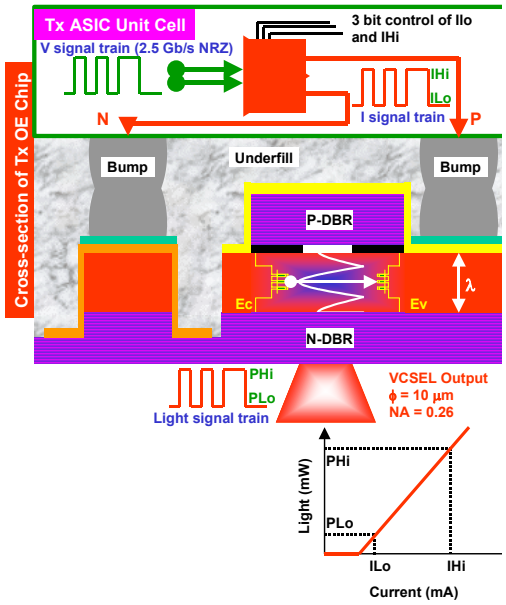

Fig. 2: Cross-section of Tx OE hybrid chip showing a backside-emitting VCSEL flip-chip-bonded to a laser diode driver (LDD) in an ASIC. The LDD converts the input voltage signal to a current signal and pumps it into the VCSEL which converts it into optical pulses. This basic unit cell can be arrayed to produce large 2DOE arrays for high-bandwidth interconnects.

component unimpeded by absorption in GaAs. The resulting Tx OE chip is schematically illustrated in Figure 2. The processing and assembly techniques we have developed produce a high yield of chips with *all 48 (or 24) VCSELs operational*. Figure 3 visually illustrates the uniformity of the output power of a 48-element VCSEL array. The threshold current at room temperature ranges from 1 to 1.5 mA, with slope efficiencies tightly clustered around a median value of at least 0.5 mW/mA. The light emitted by the VCSELs is collected by an ordered array of optical waveguides terminated in standard MPO connectors secured to the module case. A similar waveguide arrangement is used at the Rx end to ferry the light to each intended detector with a crosstalk figure less than –25 dB. In keeping with the fact that detectors are more forgiving semiconductor components than semiconductor lasers, the yield of Rx OE chips is generally even higher than that of their Tx counterparts.

One of the principal advantages of the flip-chip bonding approach is to keep the length of the electrical interconnects between active device (VCSEL or detector) and ASIC down to a minimum. Parasitics are thereby minimized, making this configuration the preferred choice to support the next generation of modules operating at data rates of 10 Gb/s and above. This advantage does, however, entail unique challenges in terms of the thermal management problem, which ultimately affects long-term device reliability and component cost. The issue is particularly critical for Tx modules. Unlike the case of top-emitting VCSELs, the heat dissipated in the active region of a bottom-emitter must first find its way to and be funneled through the nearest interconnect bump, which constitutes the primary thermal bottleneck. By resorting to larger bumps positioned as close to the emitting region as possible, we have succeeded in reducing the thermal resistance to as low as 1900 C/W, almost on a par with typical top-emitters. In a hybridized configuration, the heat dissipated in the active layer of any one VCSEL must be disposed of in two stages: First though the metal bumps, and second through the support medium to which the array is flip-chipped (ASIC in the case of an OE chip or silicon fan out such as is typically used in life test experiments). The support medium contributes a small additional resistance (10 to 20 C/W, depending on the surrounding airflow) to the overall thermal path.

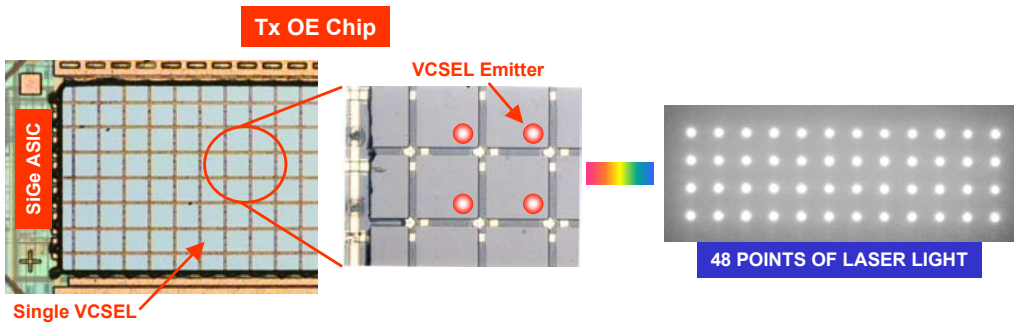

Fig. 3: Top-view of a 6x12 array of VCSELs hybridized to a SiGe ASIC (left) with a closeup (middle) showing the location of the laser cavity in the unit cell. The center 4x12 portion of the array is turned on to emit 48 multi-mode laser beams at ~ 850 nm (right) on 125x125 μm pitch.

This additional resistance is completely negligible when dealing with a single VCSEL. It can, however, add up to an appreciable extra temperature rise when *all* members of a 2D arrays are powered. Finally, the ASIC is itself an active component which generates heat of its own. Good design practice dictates that the heat-producing regions be segregated as far away from the VCSELs' light-emitting areas as is practical (avoid placing the VCSEL emitter on top of a "hot plate").

RELIABILITY

The reliability demands placed on a 2D transmit module are notably more stringent than for an individual emitter inasmuch as an entire module must be replaced as soon as the first element of the array fails (or, preferably, when it is about to fail). The expected time to failure of the first element in a cluster of 48 is of necessity shorter than the life expectancy of a single device of similar design and characteristics. The point is illustrated in Figure 4, which assumes that individual devices obey a lognormal failure probability distribution function (pdf). The median life of the parent population shown in Figure 4 has been scaled to peak at 1 hour, with a standard deviation σ of 0.7. Note that the pdf applicable to the *first* failure (leftmost histogram) is slightly skewed and peaks at a shorter time, although it is more tightly clustered in time than the pdf of the parent population.

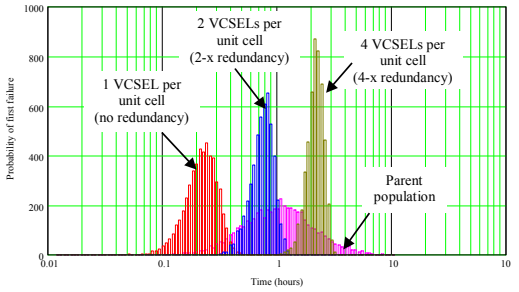

Fig. 4: Benefits of redundancy in a 4x12 array as measured by histograms of first failures in a group of 48 elements. The life expectancy of a 4x12 module with 2-x redundancy is almost the same as the median life of individual VCSELs under like operating conditions.

A very effective way to increase array longevity is to incorporate one (or more) spare VCSELs per unit cell. The spares must be physically located in close proximity to the primary VCSEL so that all members of a cluster can couple efficiently into a common fiber pigtail or waveguide. The criterion for module failure becomes synonymous with the first occurrence of failure of the *last available spare* in any one of the 48 unit cells. Figure 4 shows the potential benefits of redundancy when implemented in a 4x12 module. Indeed, our analysis indicates that the lifetime of a 4x12 transmit module with 2-x redundancy can exceed that of the current industry-standard 1x12 arrays. This advantage comes at the cost of some increased complexity of the ASIC, which must now include the functional features enabling it to recognize that a primary VCSEL is about to fail in a particular unit cell and to switch to a backup with no service interruption. In turn, this implies the ability to monitor the average power output of individual VCSELs constituting the 2-D array. Such "smart" ASICs are currently under development.

The parameter of utmost relevance to system engineers when specifying the reliability of an optical link is the FIT rate. A commonly stated aim is to maintain a FIT rate under 100 hours^{-1} over a 10-year life span of the hardware involved—an ambitious goal considering that the case temperature is allowed to reach 85°C. The FIT rate corresponding to a lognormal pdf is a strong function of time (only in the case of an exponential pdf is the FIT rate a constant in time). The relevant question to ask may then be articulated as follows: If the FIT rate of the transmit module is to remain below 100 hours^{-1} out to 10 years of operation (meaning that of 10^9 modules surviving to the 10-year mark, no more than 100 can fail during the next hour) under a particular set of operating conditions, what must the median life of that part be under those operating conditions? For a distribution of the type shown in Figure 4, the answer is roughly 25 years, which implies a median life for *individual* devices of 100 years. Recent advances in VCSEL technology have made such longevities achievable.[1],[2] As usual, life expectancies are reduced at higher drive currents I (as $1/I^2$) and at higher junction temperatures T_j [as $\exp(E_a/kT_j)$, where E_a is the activation energy].

All these considerations can be used to predict the FIT rate of a 2-D transmit module at a particular time into its useful life as a function of key operating parameters such as average drive current and case temperature. Figure 5 displays the result of such an exercise, assuming that our VCSELs are operated at an average current of

4.5 mA. The calculations suggest that 2-x redundancy (T48-gen2) is required if the FIT rate of a 48-channel module is to be kept below 100 hours^{-1} at a case temperature near 85ºC, whereas in the absence of redundancy the case temperature should not exceed 60ºC. For comparison purposes, Figure 5 also shows curves calculated for a conventional 1x12 linear array, as well as for a 4x12 array mated to an improved ASIC generating less heat.

This analysis is based on several underlying assumptions. At the component level, the processing steps used to fabricate O-E chips do not introduce new failure modes inherent to hybridization. Furthermore, the mechanical and optical designs of modules are robust enough to ensure that the coupling efficiency of the VCSEL output beams into their respective waveguides is stable in time. Finally, a background of random failures has an associated FIT rate (constant in time) which is expected to be well below the 100-hours^{-1} level.

We are currently conducting accelerated life tests of 2D arrays hybridized to fan-outs under various current and temperature operating conditions. Hybridized VCSEL arrays are being powered in burn-in ovens and given periodic check-ups at ambient temperature. Figure 5 shows the status of one 4x12 array run at 100°C chamber temperature with 3 mA of dc current per channel (corresponding to about 1 mW output power at room temperature). Since no failure has occurred to date in over 58,000 device-hours, actual FIT rates cannot be determined as of yet. Reliability tests are ongoing.

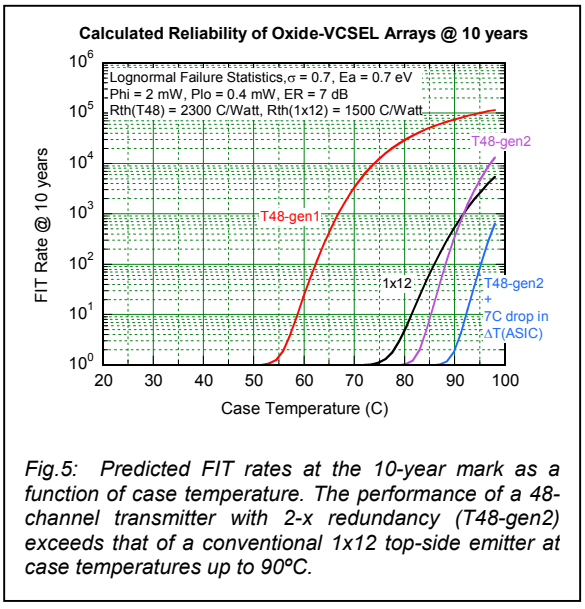

Fig.5: Predicted FIT rates at the 10-year mark as a function of case temperature. The performance of a 48-channel transmitter with 2-x redundancy (T48-gen2) exceeds that of a conventional 1x12 top-side emitter at case temperatures up to 90ºC.

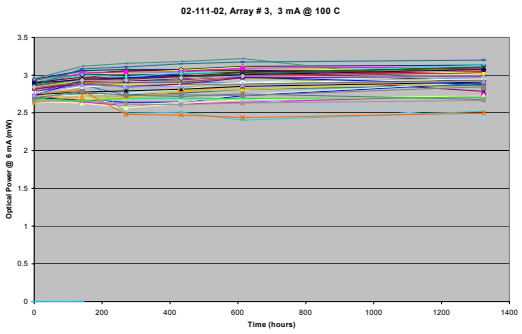

Fig. 6: Degradation trend of a 4x12 VCSEL array hybridized to a fan out. The array is being run in an oven maintained at a temperature of 100°C, with 3 mA of dc current flowing through each VCSEL. The metric used to monitor the health of a module is the power output of each VCSEL at a current of 6 mA at room temperature.

CONCLUSIONS

These preliminary results demonstrate that our processing and assembly technology is capable of producing OE modules that are rugged and reliable. These modules are poised to become legitimate contenders for insertion into commercial systems.

REFERENCES

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ACRONYMS

VCSEL: Vertical Cavity Surface Emitter
Tx: Transmitter
Rx: Receiver
OE: Opto-Electronic
ASIC: Application Specific Integrated Circuit
FIT: Failure Unit (1 FIT = 1 failure in 10^9 device-hours)

