

Power GaInP/GaAs HBTs for High Voltage Operation

P. Kurpas, A. Maaßdorf, W. Doser*, W. Köhler, P. Heymann, B. Janke, F. Schnieder, H. Blanck*, P. Auxemery**, D. Pons**, W. Heinrich, J. Würfl

Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH)

Albert-Einstein-Str. 11, 12489 Berlin, Germany

Phone: +49-30-6392-2674, fax: +49-30-6392-2685, e-mail: kurpas@fbh-berlin.de

* United Monolithic Semiconductors GmbH, Wilhelm-Runge-Str. 11, 89081 Ulm, Germany

Phone: +49-731-505-3097, Fax: +49-731-505-3005, e-mail: doser@ums-ulm.de

** United Monolithic Semiconductors S.A.S., Route Departementale 128, 91401 Orsay, France

Phone: +33-1-69330212, Fax: +33-1-69330203, e-mail: dominique.pons@ums-gaas.com

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Abstract

We report on GaInP/GaAs HBTs tuned for operation at high bias voltage as commonly used for base station amplifiers. These devices deliver up to 10 W at 26 V and 2 GHz. Their ruggedness is demonstrated by operation up to 36 V, where still 6 W output power is obtained despite of very high dissipated power of ~ 9 W. The power performance of these HBTs is limited by heatsinking conditions. Conventional backside soldering on a heatsink is compared with flip-chip soldering on AlN submount as developed at FBH. The superiority of flip-chip mounting is predicted by thermal simulations and confirmed by increased output power, higher efficiency and higher gain. Especially, PAE up to 83 % and 15 dB gain were measured on flip-chip mounted HBTs delivering 5.5 W of output power.

INTRODUCTION

GaInP/GaAs heterojunction bipolar transistors (HBTs) are well suited for power applications in mobile communications as documented by their market share for cellular handsets. The key advantages of HBTs: high efficiency and high linearity, make them promising competitors with LDMOS power devices for base station amplifiers. Especially, the high output impedance of HBTs allows easier combining to large power cells [1]. Furthermore, HBTs have the potential for high power operation in much wider frequency bands above 3 GHz as compared with LDMOS.

In this paper we report on GaInP/GaAs HBT power cells, which have been shown to operate at bias voltages higher than 26 V [1]. A further improvement in HBT performance is achieved by optimizing heatsinking of these high power devices.

EXPERIMENTAL

The high voltage HBT structures (HV-HBTs) are grown in-house on 100 mm GaAs substrates in an Aixtron AIX2400 PlanetaryTM MOVPE reactor. The layer structures mainly consist of a 700 nm GaAs subcollector layer ($n=5 \times 10^{18} \text{ cm}^{-3}$), an up to 3500 nm thick GaAs collector layer (lowly doped in a region of $4 - 6 \times 10^{15} \text{ cm}^{-3}$), a 100 nm GaAs base layer ($p=4 \times 10^{19} \text{ cm}^{-3}$), a 40 nm $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ emitter layer ($n=5 \times 10^{17} \text{ cm}^{-3}$), and GaAs and InGaAs contact layers. Si and C are used for the n-type and p-type doping, respectively. Higher resistance layers are included in the HBT structure as emitter ballast in order to increase the electrical and thermal stability of the device. The HBT process technology is based on a two-mesa approach in order to access the base and the collector layers. Interconnections are made by Ti/Pt/Au metal and emitter thermal shunts are formed by a 20 μm thick electroplated Au layer which is well visible in Fig. 1.

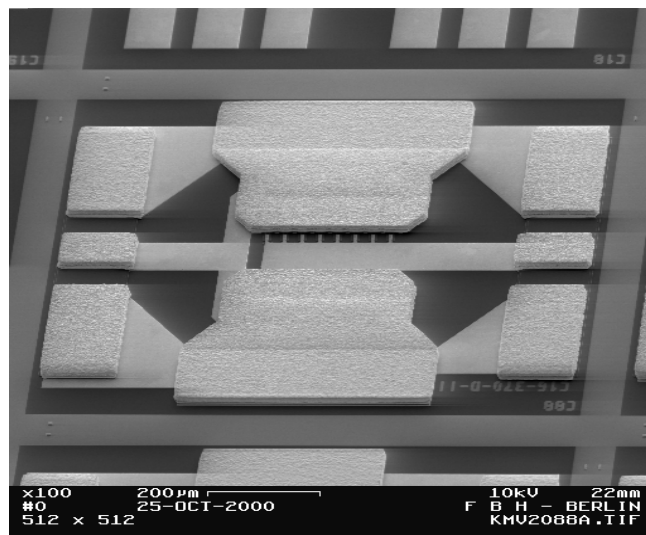


Fig. 1: SEM image of HBT power cell.

The technology challenge caused by the very high device topography of $\sim 5 \mu\text{m}$ were already described elsewhere [2]. As we do not use any planarization after etching the very thick collector layer, we developed a $10 \mu\text{m}$ BCB technology in order to increase mechanical stability of the thermal shunt bridges. After frontside processing the HBT wafers are thinned to a total thickness of $100 \mu\text{m}$. The backend process is completed by $30 \mu\text{m}$ via-hole etching and backside metallization.

HBT single devices with an emitter area of $3 \times 30 \mu\text{m}^2$ as well as power cells with up to 24 emitter fingers and a total emitter area of $5040 \mu\text{m}^2$ were fabricated (Fig. 1). The power performance is characterized by load-pull measurements under class B conditions at 2 GHz.

ON-WAFER POWER MEASUREMENTS

Power measurements are routinely performed just after the frontside processing. Fig. 2 shows that quite high output power levels of 6.2 - 7.8 W for the $3360 \mu\text{m}^2$ devices can be reached already on the unthinned substrate. After thinning to $100 \mu\text{m}$ and completing the backend process a quarter of this HBT wafer was put on an Al plate using thermal grease between wafer and heatsink. This preliminary "mounting" improves the output power to 8.8 W for the $3360 \mu\text{m}^2$ HBT as shown in Fig. 2. The larger devices were also measurable delivering now up to 9.8 W for the $5040 \mu\text{m}^2$ power cell. Smaller HBTs with emitter areas $< 3000 \mu\text{m}^2$ show almost linear dependence between output power and emitter area. However, for larger devices the power density decreases from 4 to $3 \text{ mW}/\mu\text{m}^2$ indicating increasing device heating with increasing area and power.

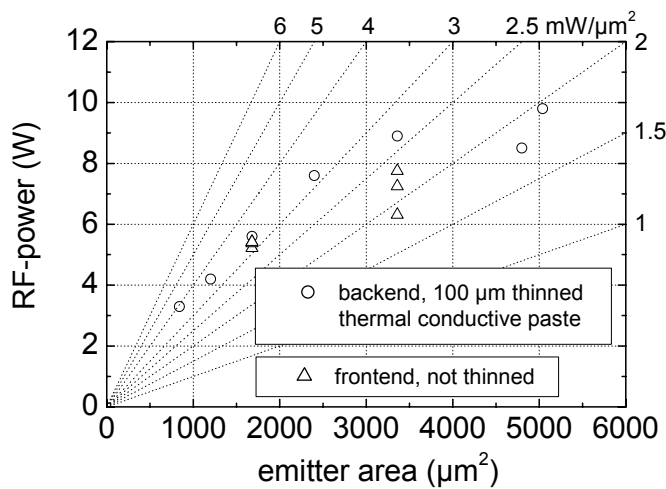


Fig. 2: Output power against total emitter area (on-wafer power measurements at 26 V bias voltage and 2 GHz on HBT wafers before and after backend processing). Dashed lines give the power densities.

The strong limitation of power by insufficient heatsinking is clearly visible for large devices $> 3000 \mu\text{m}^2$ where the output power saturates at the 10 W level. Regarding the RF performance, a power added efficiencies PAE of 70 % and 50 %, and a gain of 11 dB for the smaller and 6 dB for the largest devices, respectively, was achieved.

HBT MOUNTING ON HEATSINK

The conventional backside soldering on a heatsink is the simplest way for HBT mounting. Fig. 3 shows a cross-section of a HBT power cell soldered on Cu heatsink. The soldering was performed using a $25 \mu\text{m}$ thick AuSn preform. Fig. 3 confirms the high soldering quality as indicated by a homogeneous thickness of the solder layer and the almost complete absence of cavities in the solder. However, the remaining solder thickness of $\sim 16 \mu\text{m}$ contributes significantly to the overall thermal resistance. A thermal resistance of $\sim 30 \text{ K}/\text{W}$ was measured on $3360 \mu\text{m}^2$ HBTs mounted in this manner.

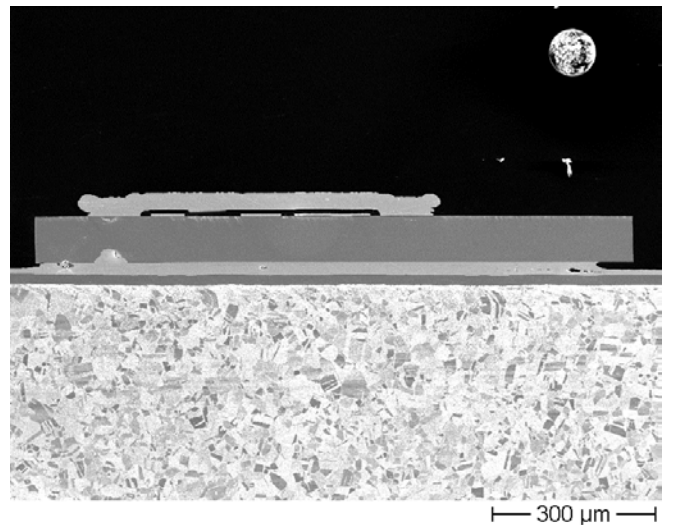


Fig. 3: Cross-section of power HBT backside soldered on Cu heatsink.

In order to evaluate the potential for heatsinking improvement thermal simulations of mounted HBT power cells were performed. Fig. 4 shows the results. Assuming an already optimized solder thickness of $7.5 \mu\text{m}$ a thermal resistance R_{th} of $\sim 19 \text{ K}/\text{W}$ can be obtained for the $100 \mu\text{m}$ thinned substrate. In the case of backside mounting a further reduction in R_{th} by 25% can be achieved only by extensive substrate thinning down to few μm . On the other hand, flip-chip HBT mounting - direct soldering on a heatsink using the Au thermal shunt bridges - gives the lowest value of thermal resistance of $14 \text{ K}/\text{W}$ in the simulation (Fig. 4). This is because, in the flip-chip case, the heatsink is located close to the heat source (collector), both being separated only by the base and emitter layers.

Accordingly, we developed a HBT flip-chip mounting process using AlN submounts with patterned Au interconnects and AuSn soldering areas. The frontside processing has to meet the requirements needed for this flip-chip mounting of HBTs. Especially, all contact areas should be on the same level as required for simultaneous soldering. We are able to equalize the emitter height by adjusting the photoresist thickness used to form the air bridges. Fig. 5 confirms that the flip-chip suited HBTs meet the tolerance of 1 μm in height deviation as required for the planar soldering. Fig. 6 shows a HBT power cell flip-chip soldered on an AlN submount. Already the first series of flip-chip mounted devices yielded high performance HBT power cells as described in the next section.

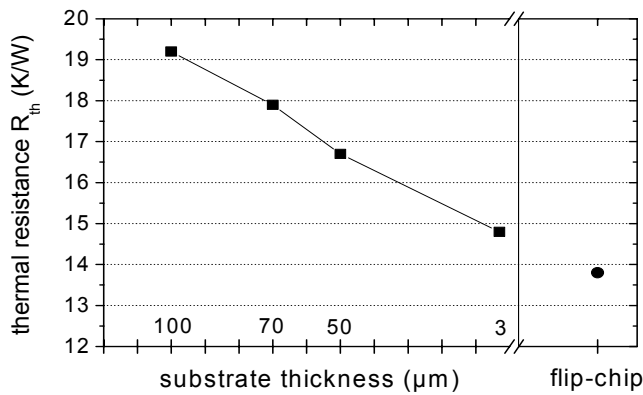


Fig. 4: Thermal resistance obtained by thermal simulations for a backside soldered HBT as a function of substrate thickness; these results are compared with calculated thermal resistance for flip-chip mounting (4000 μm^2 total emitter area in all cases).

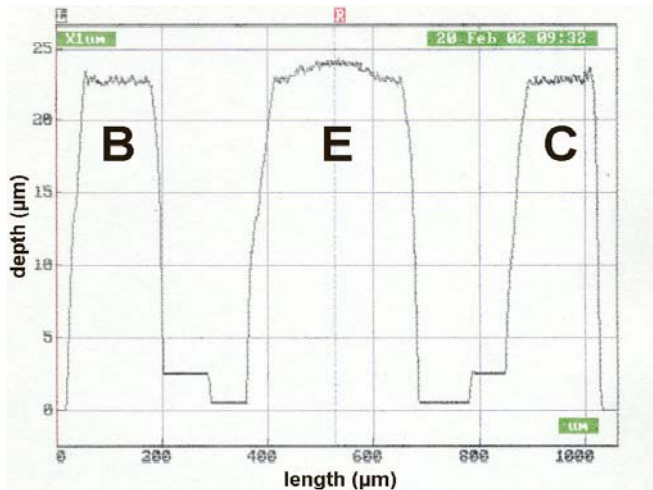


Fig. 5: Depth profile on HBT chip prepared for flip-chip mounting (B: base, E: emitter, C: collector contacts).

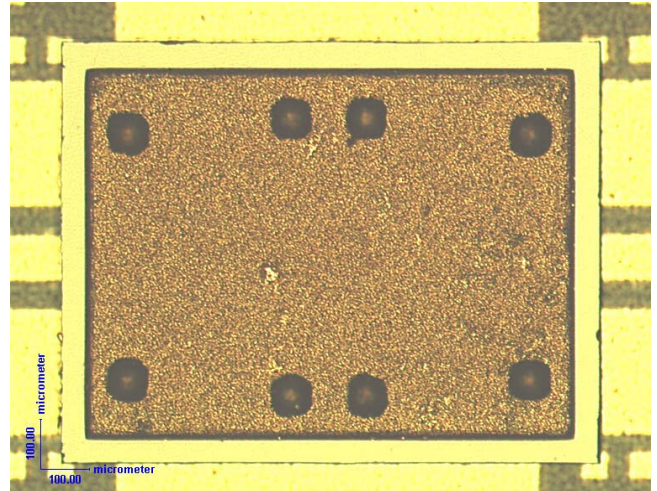


Fig. 6: Top view of HBT power cell flip-chip soldered on AlN submount.

POWER MEASUREMENTS ON MOUNTED DEVICES

After mounting the HBT power cells can be driven to higher power levels and higher operating voltages due to the improved heatsinking conditions. Fig. 7 shows the typical power performance as a function of bias voltage. A wide maximum in output power of 8.5 W and in gain of 11 dB was observed in the voltage range of 26 - 31 V for this device. At higher voltages output power and gain decrease. This is caused by increasing device temperature since the dissipated power continuously increases with increasing operating voltage. As a result, the power added efficiency decreases from 58 % at 26 V to a value below 40 % at 36 V. However, the HBT power cell still delivers high output power of 6.3 W at 36 V despite of the very high dissipated power of 8.8 W. This result highlights the robustness of our HBT devices.

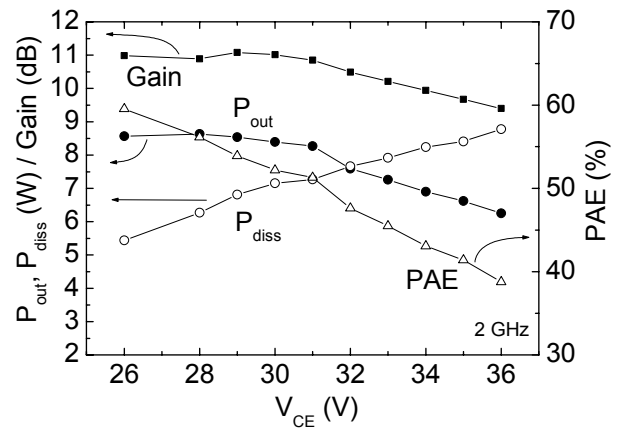


Fig. 7: Measured output (P_{out}) and dissipated (P_{diss}) power, power added efficiency (PAE) and gain of 3360 μm^2 HBT power cell against bias voltage V_{CE} (HBT backside soldered on Cu heatsink).

In Fig. 8 power results from mounted devices are compared with results obtained by on-wafer measurements (Fig. 2). The improvement by the mounting is confirmed by the result that the power level of nearly 10 W can be achieved now using HBT power cells of $3360 \mu\text{m}^2$, which is significantly smaller than in the on-wafer case. Even the performance of the $1680 \mu\text{m}^2$ devices is improved after mounting despite of the fact that they are already working at very high power density of more than $3 \text{ mW}/\text{mm}^2$. Fig. 9 shows the power results from the $1680 \mu\text{m}^2$ HBT cells in detail for all four heatsinking conditions discussed before. The superiority of the flip-chip mounting is clearly visible in this case: these devices deliver the highest output powers, and they reach or even exceed the 6 W power level. However, the advantages of flip-chip mounting are not as clear for the first mounting test of larger HBTs of $3360 \mu\text{m}^2$ emitter area (see Fig. 8). This indicates that further optimization of the flip-chip soldering is needed especially for large emitter area HBTs.

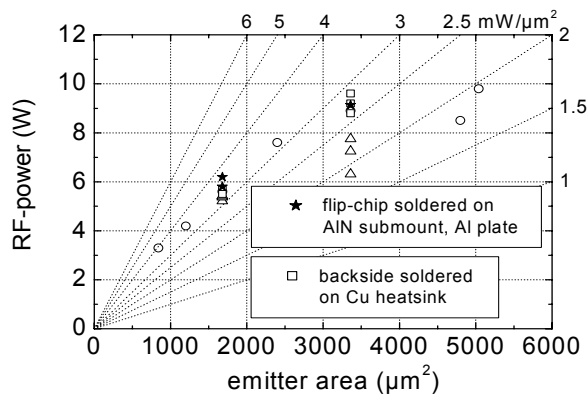


Fig. 8: Output power of heatsink-mounted HBT power cells as a function of emitter area (26 V, 2 GHz). Results from on-wafer measurements (Fig. 2) are included.

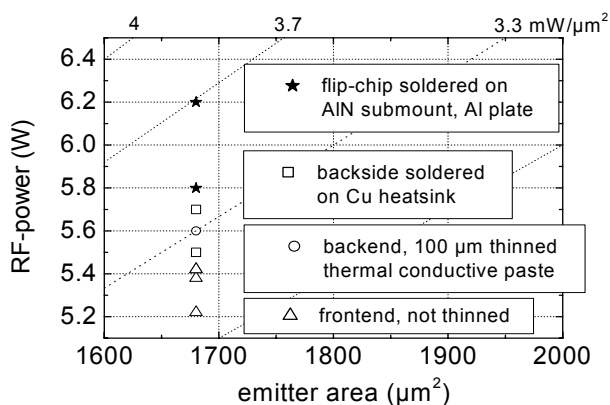


Fig. 9: Output power delivered by $1680 \mu\text{m}^2$ HBT power cells under different heatsinking conditions (detail of Fig. 8).

Fig. 10 provides additional data on the advantage of flip-chip mounted HBT power cells as compared with backside soldered devices taken from the same wafer. As can be seen, the flip-chip soldered HBTs exhibit both highest gain in the order of 15 dB and highest efficiencies of 74 - 83 %.

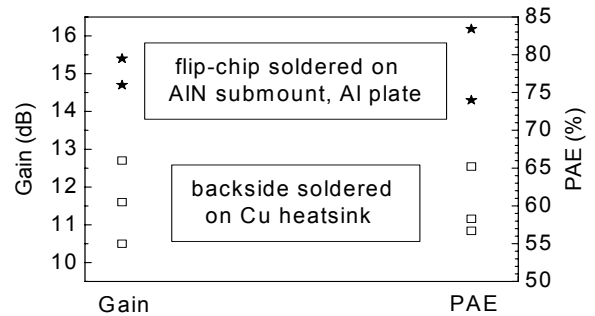


Fig. 10: Comparison of flip-chip mounted and backside soldered HBT power cells in terms of gain and PAE ($1680 \mu\text{m}^2$ HBT, 26 V, 2 GHz).

CONCLUSIONS

GaInP/GaAs HBTs prove to be suitable for high power applications at high voltages. Operation at bias voltages as high as 36 V and high output power levels of 5 - 10 W confirm the good intrinsic performance of the HBT power cells. Efficient heatsinking is crucial to achieve full device performance. Flip-chip mounting is shown to be the preferable way for thermal stabilization. Additional improvements of available output power can be expected after further optimization of flip-chip mounting of large HBT power cells.

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ACRONYMS

HBTs: Heterojunction Bipolar Transistors
PAE: Power Added Efficiency