# Refractory Gate Metallization Characterization for HIGFET Power Amplifiers

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## Abstract

**HIGFET or Enhancement Mode Off-State Leakage ($I_{off}$) unit probe specification was tightened significantly in early 2002 for a wireless telephone platform, causing a need for additional characterization of related process modules. Results of an effort to further characterize the E-mode gate metallization process and its effects on $I_{off}$ are reported. Effects of controlled process inputs and uncontrolled deposition system parameters on key film and device electrical parameters, including $I_{off}$, are analyzed. Moreover, efforts to eliminate gate metal delamination are presented. All these efforts resulted in a reduction in variation of up to 35% (wafer-to-wafer) for several film and device electrical parameters.**

## INTRODUCTION

The reduction of $I_{off}$ unit probe specification led to an effort to further characterize many processes within the E-mode process flow. Among those thought to have a contribution to leakage was the TiWN refractory gate metallization process. This paper presents findings regarding the effects of deposition pod temperature equilibrium on within lot film and electrical parameter variation. In addition, results from a fractional factorial designed experiment, which was conducted to understand effects of main process inputs on device electrical performance are presented. Finally the effects of TiWN film stress on adhesion is demonstrated.

## CHAMBER CONDITIONING

The uncontrolled heating of the deposition chamber during system operation significantly contributes to poor process control of several film properties and, as a result, device parameters. As wafers are run through a deposition cycle the system's shielding temperature increases due to heat transfer from the sputtering plasma. Thermocouple measurements indicate that the shield temperature does not reach thermal equilibrium until nearly a full cassette of 25 wafers has been processed. Figure 1 indicates that as wafers are processed through the system the temperature of the shield closely correlates to the increasing sheet resistance of the film.

Heat contributed to the process from the shields decreases the deposition rate (Figure 2) and increases the amount of $N_2$ incorporated into the film (Figure 3). The phenomenon exhibits itself as increasing Gate Metal Sheet Resistance as sequential wafers are processed until thermal equilibrium of the shielding has been achieved.

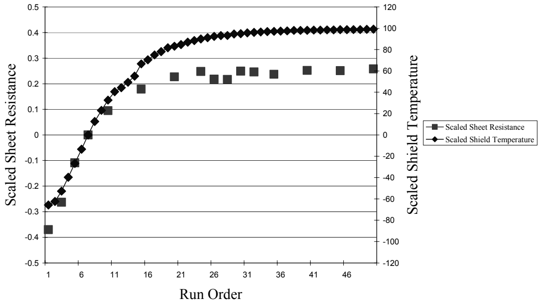

Figure 1 - Shield Temperature and Film Sheet Resistance Correlation

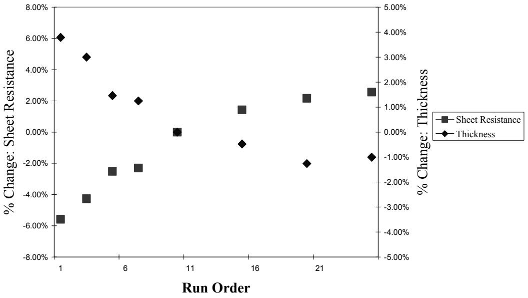

Figure 2 - Shield Temperature Effect on Film Sheet Resistance/ Thickness

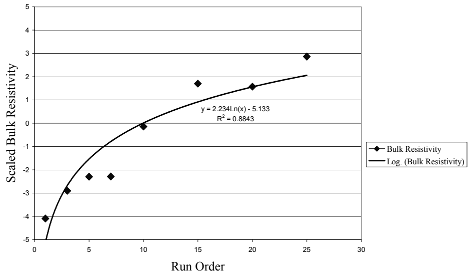

Figure 3 - TiWN Bulk Resistivity Vs Run Order

Preconditioning the deposition system prior to committing production material brings the shielding to thermal equilibrium thus ensuring that all wafers within a lot are exposed to consistent process conditions. Figure 4 demonstrates the effects of chamber pre-conditioning on TiWN sheet resistance.

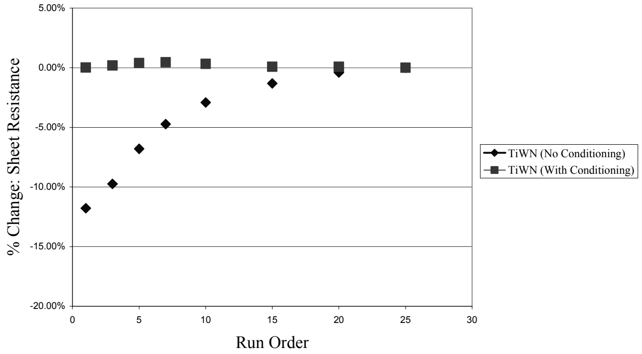

Figure 4 - Impact of Conditioning on Sheet Resistance

Implementation of deposition chamber pre-conditioning resulted in a reduction in within-lot variation of several device electrical parameters (Table 1) [2].

Table 1. Reduction in TiWN Related Device Electrical Parameters Using Pre-Conditioning

| Device Parameter | Reduction Realized |
|---|---|
| Off-State Leakage Current | 35% |
| TiWN Sheet Resistance | 10% |
| Gate Length | 10% |
| Threshold Voltage | 5% |

## DESIGNED EXPERIMENT

Once the effectiveness of pre-conditioning had been demonstrated, additional characterization work on controlled process parameters was undertaken. A fractional factorial designed experiment was conducted to further understand the effects of controlled process inputs on electrical device performance. Experimental factors selected for the study were; $N_2$ flow, Ar flow, throttle valve position, deposition power and back plane temperature. Table 2 lists the responses in order of statistical significance to the factors in the experimental model.

As indicated in the table, many responses not intuitively associated with the TiWN process have no significant impact on gate-related device performance. Of interest is the fact that with chamber conditioning, $I_{off}$ does not indicate statistical significance.

Table 2. Analysis of Variance: TiWN DOE Results

| Response | Best Fit R2 | Best Fit Adjusted R2 | ANOVA F | Lack of Fit MaxR2 |
|---|---|---|---|---|
| TiWN Sheet Rho | 0.943 | 0.942 | 0.0001 | 0.943 |
| Gate Length | 0.78 | 0.775 | 0.0001 | 0.81 |
| Drain Current | 0.754 | 0.747 | 0.0001 | 0.759 |
| Threshold Voltage | 0.689 | 0.683 | 0.0001 | 0.691 |
| Gate-Source Breakdown | 0.628 | 0.619 | 0.0001 | 0.649 |
| On Resistance | 0.583 | 0.57 | 0.0001 | 0.593 |
| Gate-Drain Breakdown | 0.574 | 0.562 | 0.0001 | 0.611 |
| Off-State Leakage | 0.447 | 0.433 | 0.0001 | 0.504 |
| On Voltage | 0.436 | 0.421 | 0.0001 | 0.48 |
| N+ Sheet Rho | 0.352 | 0.338 | 0.0001 | 0.389 |
| Contact Resistance | 0.245 | 0.226 | 0.0001 | 0.277 |
| N- Sheet Rho | 0.233 | 0.221 | 0.0001 | 0.309 |
| Capacitance | 0.032 | 0.022 | 0.006 | 0.077 |

Different experimental factor combinations in effect change the gas residence time in the system and create the wide range of bulk values shown in Figure 5. For example: low deposition rate and high $N_2$ flow increases the film bulk resistivity. When Figure 5 is compared to Figure 6, it is clear that bulk values outside a nominal range influence device electrical performance. Drain current (Figure 6) is the only electrical parameter presented here but several other electrical parameters exhibited the same behavior. The findings were useful in defining a process window for TiWN bulk resistivity, which is limited by device resistor requirements.

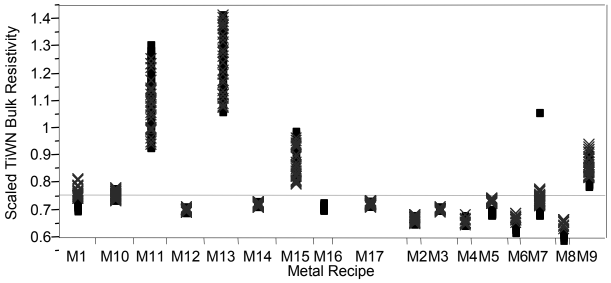

Figure 5 - TiWN Bulk Resistivity by Deposition Process

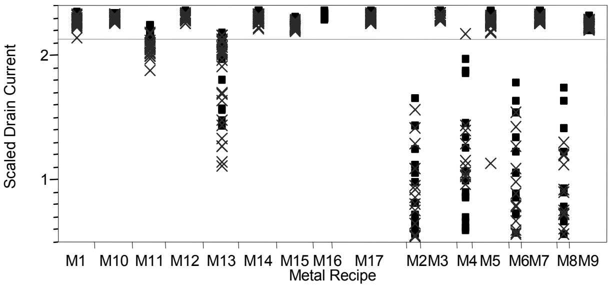

Figure 6 - Device Drain Current by Deposition Process

The designed experiment indicated that TiWN bulk resistivity influenced several device electrical parameters. However, process input variations are controllable such that operation within the acceptable process window is easily maintained. In this case, existing process input variations are shown to be non-critical with respect to process control. The designed experiment showed that a change in the present process input levels or machine configuration was not necessary.

## FILM STRESS and ADHESION

TiWN film de-lamination from the GaAs substrates not only results in yield loss, but also particle contamination of down stream tools. A reduction in film thickness or stress is necessary to reduce the probability of film de-lamination. These two parameters are related algebraically through the following equation where Z is a dimensionless cracking parameter, $s_R$ is the residual stress in the film, h is the film thickness and E is the Young's Modulus [1].

$$G=(Zs_R^2h)/E$$

Theoretically if the energy release rate of a crack in a film is greater than the interfacial fracture toughness, de-lamination can occur. Highly compressive residual stress in films, such as the TiWN film shown in Figure 7, can result in film buckling known as "telephone cord" de-lamination.

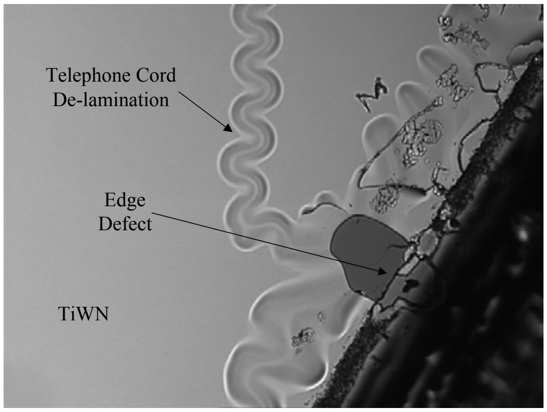

Figure 7 - Micrograph of Delaminating TiWN Film

After the film is deposited, the wafers travel through several downstream processes before the majority of the film is etched away. During that time, the TiWN film on the wafer edges comes into physical contact with cassettes, a variety of wafer handling systems and equipment such as wet clean tools. This contact creates micro cracks in the film thus initiating "telephone cord" de-lamination (Figure 8).

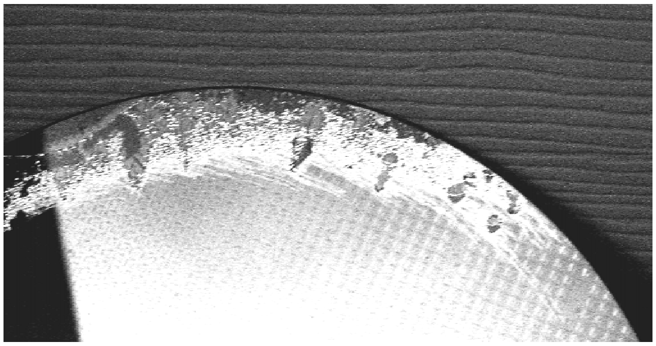

Figure 8 - Radial Propagation of Telephone Cord De-lamination

The cords then propagate along the most highly stressed area of the film. Residual stress maps of the TiWN film (Figure 9) show that the most highly stressed area of the film is along the outside edge, which is why the cords propagate radially and stay at the edge of the wafer as seen in Figure 8.

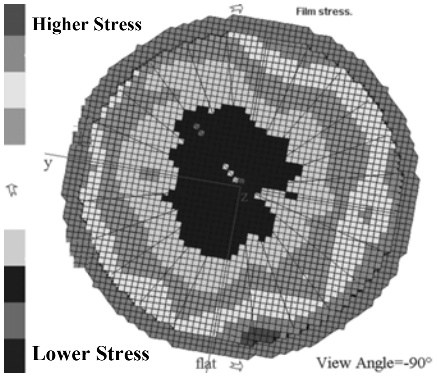

Figure 9 - Stress Map of TiWN Gate Metal on GaAs

Two approaches were examined to eliminate "telephone cord" de-lamination. The first was to reduce over-all film stress. By manipulating the point of entry (POE) of process gases the stress of the film was reduced by a factor of 10 (Figure 10).

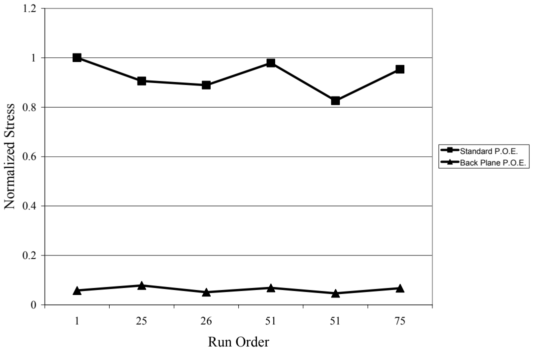

Figure 10 - Normalized TiWN Stress vs. Process Gas P.O.E.

The second approach was to mask the edge of the wafer during deposition using a modified wafer holder thus avoiding physical damage of the film. Even if the TiWN film is highly stressed, it will not delaminate unless it is initially damaged by physical contact. By masking the edge of the wafer during deposition, the film is not subjected to physical damage from downstream processing and therefor does not de-laminate. Figure 11 shows micrographs of wafers with and without edge exclusion at TiWN deposition.

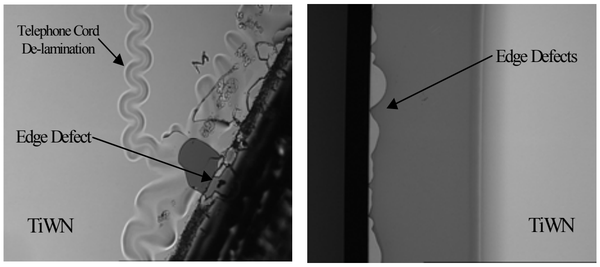

Figure 11 - Optical Micrographs of Wafers With/Without Edge Exclusion

## Conclusions

The process improvements and characterization documented here have resulted in a robust TiWN metallization process. The implementation of chamber conditioning has increased process capability to well above six sigma levels, reduced variation in device parameters, reduced scrap due to that variation, and has provided confidence in further characterization of the gatemetal. The designed experiment conducted for purpose of characterizing the effects of device parameters as a function of TiWN process inputs defined a usable specification window. Finally, the work surrounding TiWN film adhesion provided avenues from which to pursue the elimination of TiWN to GaAs film de-lamination.

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## References

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## Acronyms

TiWN- Titanium Tungsten Nitride
$I_{off}$- Off State Leakage Current
POE- Point of Entry
E-mode – Enhancement Mode