Trade-off Relationship between Breakdown and Gate-Lag in Recessed-Gate GaAs FETs

Y. Mitani, D. Kasai and K. Horio

Faculty of Systems Engineering, Shibaura Institute of Technology
307 Fukasaku, Saitama 330-8570, Japan (E-mail: horio@sic.shibaura-it.ac.jp, TEL: +81-48-687-5813)

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Abstract

Breakdown characteristics of recessed-gate GaAs MESFETs are studied by two-dimensional analysis including surface states and impact ionization of carriers. It is shown that the breakdown voltage could be rather lowered when introducing a narrowly-recessed-gate structure. Recess-parameter dependence of gate-lag (or slow current transients during turn-on) is also analyzed. It is shown that there may be a trade-off relationship between raising the breakdown voltage and reducing the gate-lag.

INTRODUCTION

Understanding high-voltage phenomena in GaAs MESFETs and HEMTs, such as drain-to-source breakdown, is very important for realizing high-performance microwave power devices and ICs, which are now receiving great interest, particularly for mobile communication applications. To achieve high breakdown voltages, so-called a recessed-gate structure has been utilized [1], where the existence of surface depletion layer due to surface states is regarded as an origin of the high breakdown voltage. On the contrary, recently, a (narrowly) recessed-gate structure is used to reduce surface-state-related anomalies such as frequency-dependent transconductance and gate-lag [2]-[4]. Considering these, it is not clear whether the recess enhances or reduces the surface-state effects.

The gate-lag in GaAs MESFETs and HEMTs is a phenomenon that the drain currents show slow transients even if the gate voltage is changed abruptly, and this is a serious problem in both digital and analog applications [2]-[5]. In digital circuits, the gate-lag results in narrowing the pulse width, finally leading to a function error. This phenomenon is problematic in digital RF systems that are pulsed on and off with short duty cycle. It is also recognized that the gate-lag is correlated to the power compression of the FETs and to the degradation of their distortion characteristics. As for the mechanism of gate-lag, effects of surface states and substrate traps are suggested, but the detailed mechanism is not well understood [6],[7].

In this work, to get a detailed insight into recess effects and surface-state effects on the breakdown and gate-lag phenomena, we have made two-dimensional analysis of recessed-gate GaAs MESFETs, in which surface states and impact ionization of carriers are included. As a result, we have found that the breakdown voltage could be rather lowered when introducing a narrowly-recessed-gate structure, and that there may be a trade-off relationship between raising the breakdown voltage and reducing the gate-lag.

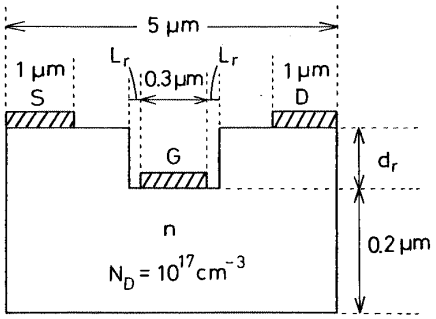
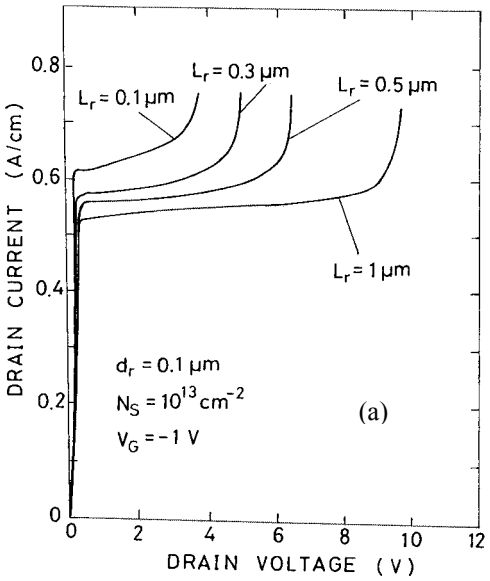


Fig.1 Modeled recessed-gate GaAs MESFET analyzed here.

PHYSICAL MODEL

Fig.1 shows a modeled device structure analyzed in this study. The surface states are considered on the planes between the source and the gate and on the planes between the gate and the drain. As a surface-state model, we adopt Spicer's unified defect model [8], and assume that the surface states consist of a pair of a deep donor and a deep acceptor. As to their energy levels, the following case, where the gate-lag was seen previously in the planar structure [6], is considered: E_{SD} = 0.87 eV, E_{SA} = 0.7 eV [9],[10]. Here E_{SD} is the energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is the energy difference between the deep acceptor's energy level and the top of valence band. The surface states are assumed to distribute uniformly within 5 Å from the surface and their densities are typically set to $2x10^{20}$ cm^{-3} (10^{13} cm^{-2}). According to previous works [4],[6], where impact ionization of carriers is not included, the deep-acceptor surface state mainly determines the surface Fermi level, and it acts as a hole trap, showing large gate-lag.



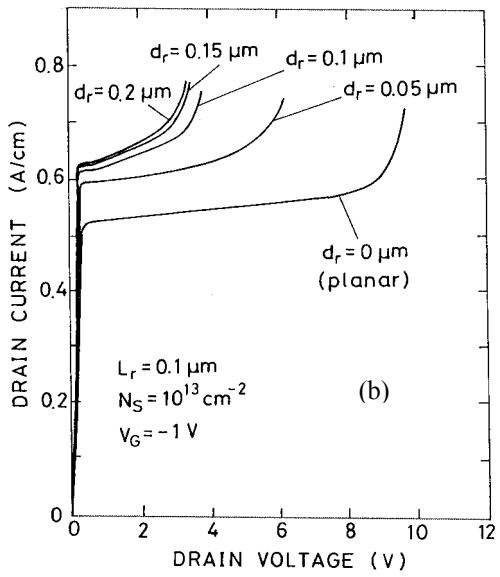


Fig.2 Calculated drain characteristics of recessed-gate GaAs MESFETs as parameters of L_r ((a)) and d_r ((b)).

Basic equations are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include a carrier generation rate by impact ionization and carrier loss rates via the deep levels, and rate equations for the deep levels. These equations are solved numerically.

BREAKDOWN CHARACTERISTICS

Fig.2 shows calculated drain characteristics of recessed-gate GaAs MESFETs (with relatively high surface-state densities of 10^{13} cm^{-2}) as parameters of the distance between the gate and the recess edge L_r ((a)) and the recess depth d_r ((b)). In Fig.2(a), d_r is set to 0.1 μm, and in Fig.2(b), L_r is set to 0.1 μm. As L_r becomes longer, steep increases in drain currents occur at higher drain voltages, that is, the breakdown voltage becomes higher, which can be naturally understood. On the other hand, we also see that as d_r becomes deeper, the breakdown voltage becomes lower than that for a planar structure (d_r = 0 μm), indicating that the breakdown voltage becomes low by introducing a recessed-gate structure. This is an unexpected result. We will discuss below why this happens.

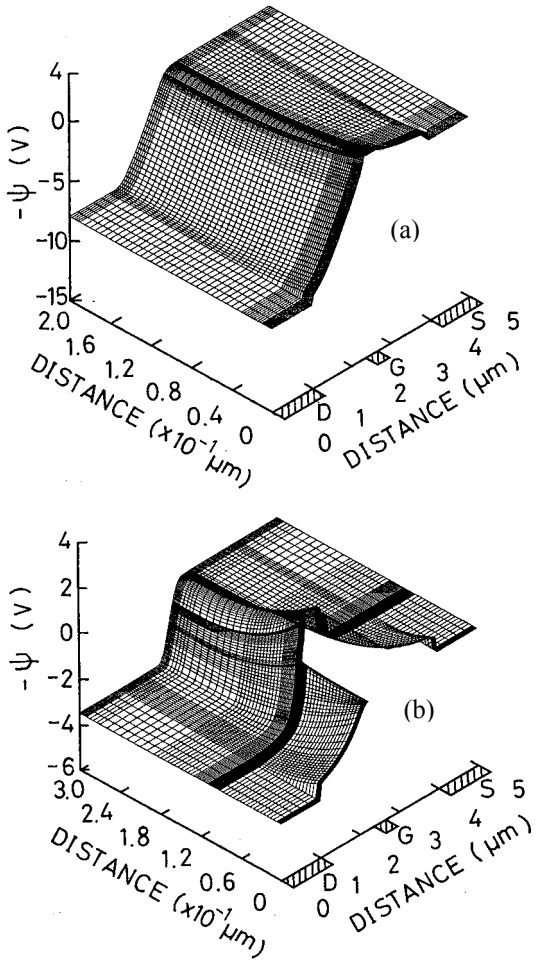
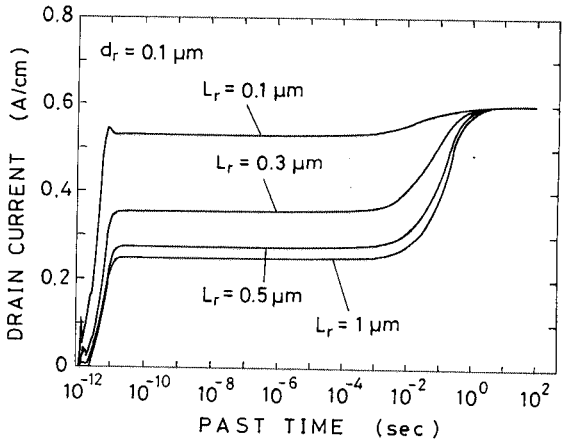
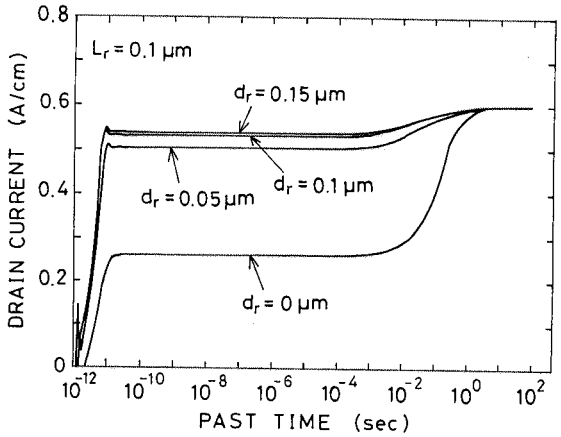


Fig.3 Comparison of potential profiles of GaAs MESFETs near breakdown. (a) planar structure (V_D = 8 V, V_G = - 1 V), and (b) recessed-gate structure with L_r = 0.1 μm and d_r = 0.1 μm (V_D = 3.5 V, V_G = - 1 V).

Fig.3 shows a comparison of potential profiles between (a) the planar structure and (b) a narrowly-recessed-gate structure (L_r = 0.1 μm, d_r = 0.1 μm). In the planar structure, the drain voltage is almost uniformly applied between the gate and the drain (1.35 μm). But in the narrowly-recessed-gate structure, the voltage drop between the gate and the recess edge (0.1 μm) is quite large, which is a cause of the lower breakdown voltage (3 ~ 4 V) in this case.



(a)



(b)

Fig.4 Calculated turn-on characteristics of recessed-gate GaAs MESFETs as parameters of L_r ((a)) and d_r ((b)).

From the above results, we can say that in the case with relatively high densities of surface states, the breakdown voltage could be drastically lowered when introducing the narrowly-recessed-gate structure.

GATE-LAG PHENOMENA

Next, we describe gate-lag phenomena. Fig.4 shows calculated turn-on characteristics of recessed-gate GaAs MESFETs as parameters of L_r ((a)) and d_r ((b)), where OFF and ON states are set so that the drain currents becomes 5x 10^{-3} A/cm and 0.6 A/cm, respectively. In Fig.4(a), d_r is set to 0.1 μm, and in Fig.4(b), L_r is set to 0.1 μm. In general, the drain currents remain low values for some periods and begin to increase slowly, showing gate-lag behavior. This is due to the slow response of surface states. This type of gate-lag is commonly seen in experiments [3]. As L_r becomes shorter, the gate-lag is reduced, because effects of surface states on the same planes as the gate electrode are reduced. As d_r becomes deeper, the gate-lag is reduced because effects of surface states on the same planes as the drain (source) electrode are reduced. But, it is not eliminated even if d_r becomes deeper than 0.1 μm, which is equal to the thickness of surface depletion layer under equilibrium. This remaining gate-lag is due to surface states on the same planes as the gate electrode. The details on the recess-parameter dependence of gate-lag were described before including effects of introducing a buried-gate structure [4], as far as a case without impact ionization was concerned.

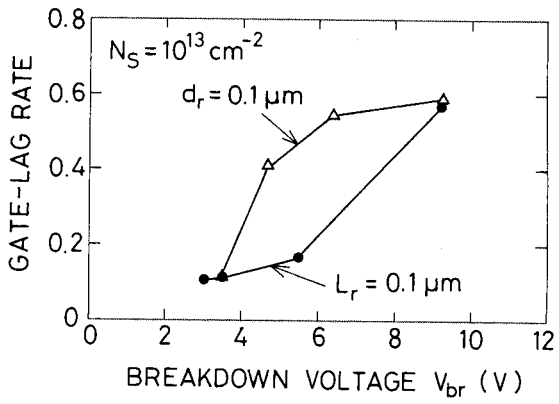


Fig.5 Relationship between gate-lag rate and breakdown voltage of recessed-gate GaAs MESFETs.

BREAKDOWN VOLTAGE AND GATE-LAG RATE

Finally, we discuss relation between the gate-lag magnitude and the breakdown voltage in the recessed-gate GaAs MESFETs.

Here, the breakdown voltage V_{br} is located at the intersection of the extrapolated saturation segment and the impact ionization induced rapidly rising segment of the *I-V* curve. And, to represent the gate-lag magnitude, we define the Lag Rate as

$$\text{Lag Rate} \equiv \frac{I_D(\text{ON}) - I_D(t = 10^{-6}\,\text{s})}{I_D(\text{ON})} \qquad (1)$$

where I_D (ON) is the drain current in the ON state, and I_D (t = 10^{-6} s) is the drain current at 10^{-6} sec after the gate voltage is switched on. The Lag Rate takes a value between 0 and 1, and a high Lag Rate means large gate-lag.

Fig.5 shows the Lag Rate versus V_{br} for the recessed-gate GaAs MESFETs, which is obtained from the data in Fig.2 and Fig.4. It is seen that there is a trade-off relationship between raising the breakdown voltage and reducing the gate-lag. This type of trade-off is also reported experimentally in PHEMTs [2].

CONCLUSION

Two-dimensional analysis of breakdown characteristics in recessed-gate GaAs MESFETs has been performed considering surface-state effects. It has been shown that in the case with relatively high densities of surface states, the breakdown voltage could be drastically lowered when introducing the narrowly-recessed-gate structure. It is suggested that there may be a trade-off relationship between raising the breakdown voltage and reducing the gate-lag.

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