

Process Optimization for 0.5 μm Dual Recess PHEMT Power Amplifiers

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ABSTRACT

The output power performance of 0.50 μm dual recessed pHEMT MMICs designed with current limited load lines strongly depends on the RF current swing of the device. What might seem a sufficient DC I_{max} of a given sample might not necessarily indicate the intrinsic output power capability of the device. The position and electrochemistry of the wide recess surface were demonstrated as important factors governing the Pout performance of TriQuint's 0.50 μm pHEMT MMICs.

This paper will describe experiments that were executed to determine the impact of wide recess position and surface treatment on the intrinsic current limited output power of a 0.50 μm PWRPHEMT device.

INTRODUCTION

Recently, double recess Pseudomorphic high electron mobility transistors (PHEMTs) have demonstrated higher performance in microwave and millimeter wave frequency ranges. The 0.5 μm power PHEMT are widely used for large power amps in the frequency range of DC to 18 GHz. The RF output power of the devices is closely related to RF I_{max} of the devices [1].

For a dual etch stop pHEMT device, we observe very consistent I_{ds} and V_p values, as one would expect for a narrow etch stop implementation for which the material parameters are sufficiently controlled. Despite the consistency of these values however, we observed significant variation in DC I_{max} values. Moreover, the variation in Pout for a particular MMIC was very pronounced. A team was formed to investigate the widely variable and lower than expected Pout responses.

At the onset certain basic assumptions were embraced. The first is that the RF I_{max} , which may or may not be strongly correlated to DC I_{max} , must be significantly dependent on the position and state of the passivated wide recess surface. It was also recognized that the state of the surface in the immediate vicinity of the gate was also very important. Furthermore, we noted that deformities of the surface, such as pits or grooves possibly introduced during certain cleanup steps, could also partly explain instances of lower than expected output power.

The first round of experiments involved asher/wet cleanup sequences at pre-passivation clean up steps. After suitable formulae were defined based on analyses of the experimental data, the focus was shifted to slight material variations to further improve the RF I_{max} . After the various experimental matrices were performed, saturated RF output power, small signal gain, and DC characteristics of MMICs and standard FET cells were analyzed as functions of the experimental factors.

DESIGN OF EXPERIMENTS

pHEMTs reported in this paper have 0.5 μm optical gates in a dual recess, double etch stop process with a source drain spacing of 3.0 μm . TriQuint manufactures both 2 and 3 level metal interconnect devices, referred to as 2MI and 3MI, in its Texas facility. In both process flows, the gate fabrication process is completed before the silicon nitride passivation of the surface. The details of the fabrication process are described in reference [2].

DC and RF characterization of the experimental devices were performed in whole wafer from a large number of samples to account for inherent process variation. The saturated drain source current, pinch-off voltage, and gate drain breakdown voltage are typically, 270 mA/mm, -1.0V, and -18V, respectively. In addition, a novel RF characterization method was developed to get rapid feedback of the impact of the process variations on the RF performance of the devices under test. Both 300 μm coplanar devices (4 X 75 μm wide gate) and 300 μm standard FET (SFC) cell devices were characterized to obtain the saturated output power at 3 GHz with a 50 Ohm load. The 300 μm co-planar device became the primary test cell because it could be measured at the end of front side processing, thus providing more rapid feedback of experimental results. Figure 1 shows the Pin/Pout characteristics of the coplanar test cell, for example:

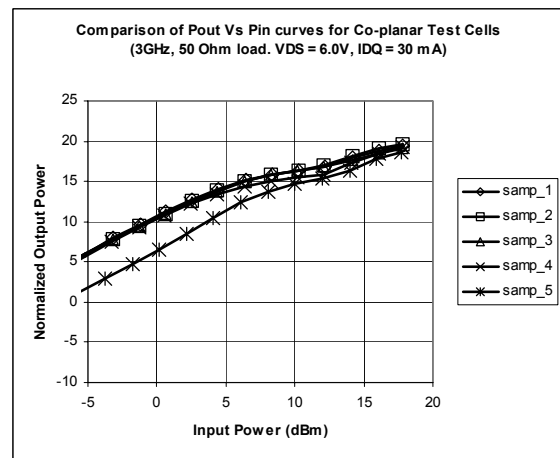


Figure 1: Pout/Pin characteristics of 300 μm co-planar FET cells with 50 Ohm load.

This remainder of this section will focus on the most informative experiments that were used to define a process for improved output power performance. The first round of experiments involved pre-passivation surface treatment of the gate channel. The following defines the factors and responses for DOE #1:

Table 1: Matrix for DOE #1

Wafer	Pre-Passivation Wet Clean	Pre-Passivation Dry Clean
1	None	None
2	PPWC A	None
3	PPWC B	None
4	PPWC C	None
5	None	PPDC A
6	PPWC A	PPDC A
7	PPWC B	PPDC A
8	PPWC C	PPDC A

Another experiment again focused on surface preparation. However, this more comprehensive matrix also focused on certain details of the gate recess processing steps. The following describes the matrix for DOE #2

Table 2: Matrix for DOE #2

Wafer	Wide Clean	Gate Lithography	Gate Recess Etch Time	Pre-Passivation
1	WC A	L1	T1	PPWC B
2	WC A	L2	T1	PPWC B
3	WC A	L2	T1	PPWC A
4	WC B	L2	T1	PPWC B
5	WC B	L2	T1	PPWC A
6	WC A	L1	T2	PPWC B
7	WC A	L1	T2	PPWC A
8	WC B	L1	T2	PPWC A

The first factor describes two different cleanup sequences following wide recess. The second describes two different patterning conditions for the gate recess. The next factor describes the etch time at gate recess. The final factor for DOE #2 describes the pre-passivation wet cleanup process variables, similar to DOE #1.

The following shows the layout of DOE #3:

Table 3: Matrix for DOE #3

Wafer	ES Position	Wide ISAT
1	X	I
2	X + 9%	I
3	X + 18%	I
4	X	I + 8%
5	X + 9%	I + 8%
6	X + 18%	I + 8%

The first factor of DOE #3 simply defines the relative etch-stop position (Schottky gate) wrt top planar doped layer. The second factor of DOE #3 defines the final wide recess target and is related

to the position of the wide surface wrt to the top planar doped layer of TriQuint's double recess pHEMT structure.

RESULTS

Once the wafers for DOE #1 completed fabrication, the standard FET cells were measured to obtain small-signal circuit parameters in a range of frequency (0.50GHz, 2-26 GHz). An equivalent extraction routine was used to obtain small signal parameters [3]. A 3.0 GHz saturated power measurement was used to obtain saturated power results in co-planar and standard FET cells. The differences in output power that were predicted by the two FET cell types were insignificant. Although the saturated power measurement is performed at low frequencies it was deemed sufficient, given an appropriate current limited load target, to highlight issues resulting from current swing. The Graphical results of DOE #1 are illustrated in figures 2 and 3 below:

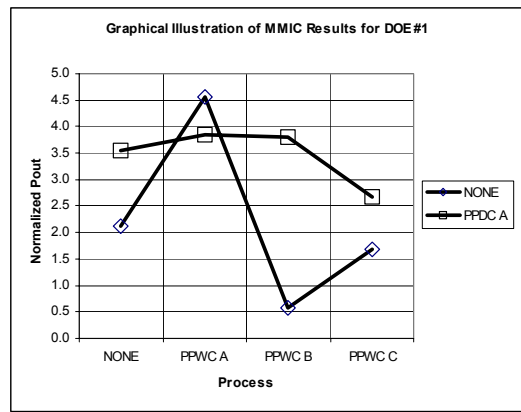


Figure 2: MMIC Psat of DOE #1 Samples

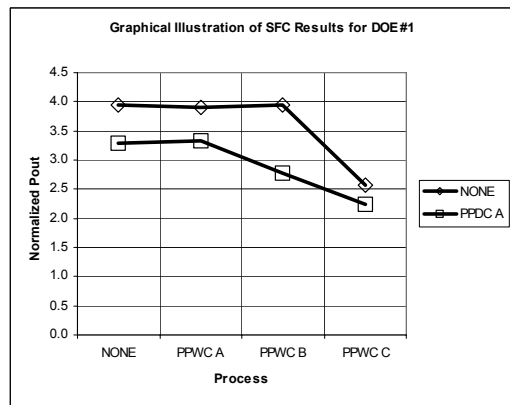


Figure 3: Psat measurements of standard cell (SFC) (DOE #1)

Figures 2 and 3 show somewhat different responses, comparing the SFC and MMIC response. The FET cell performed better with no dry clean step, while the MMIC power was better, for most legs, when the dry clean was included. The dry clean was later deemed necessary for unrelated process reasons. Among the DOE legs including the dry clean, the pre-passivation wet clean sequence PPWC A gave the best power performance for both MMIC and SFC.

The following figure shows response plots for DOE #2 (described in previous section) which illustrate the relative effects of each of the 4 input variables on the pout response:

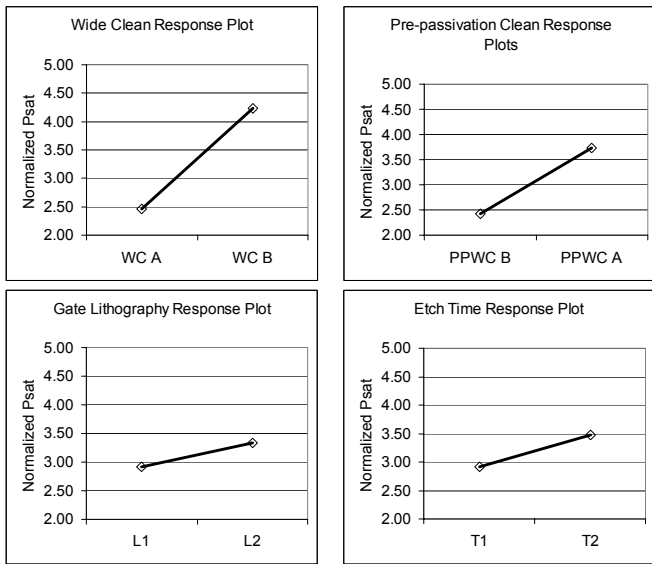


Figure 4: Output power response plots for DOE #2 from SFC test structures

According to the response plots in figure 4, the wide recess cleanup sequence and the pre-passivation wet clean are the most significant factors in terms of the effect on Psat as measured on standard cell devices. The wide cleanup sequence WC B and the pre-passivation cleanup PPWC B were implemented into the improved process flow.

The following scatter plot illustrates the outcome of DOE #3:

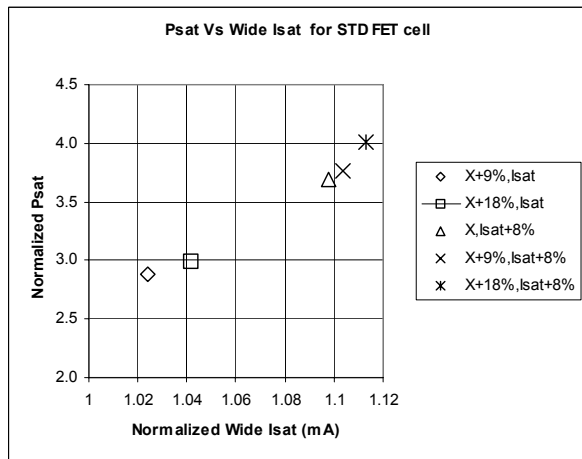


Figure 5: Co-planar Psat Vs Wide Isat of DOE #3 Results

The two primary factors considered in DOE #3 were narrow etch-stop position and wide recess Isat. A brief study of the figure above shows that the bigger effect is final wide recess Isat current as indicated by the separation between the two clusters of points as

compared to the separation of points within any of the two clusters. Further consideration of the results lead to the conclusion not to implement the material etch-stop change as an option because of some risk of altering equivalent circuit parameters. The following graph illustrates the impact of material and wide Isat on RF Gm, for example:

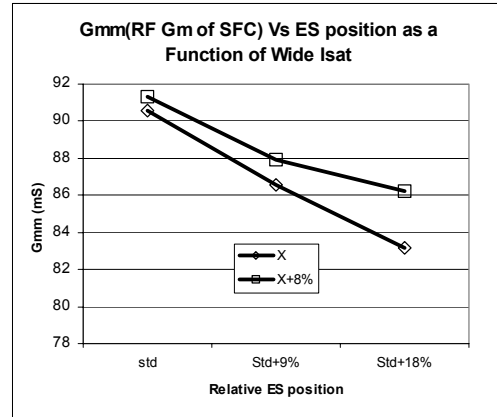


Figure 6: Extracted RF Gm (Vd= 8V, Idq= 75 mA/mm) Vs ES position as a function of wide recess Isat.

The graph shows that there is very little change in RF Gm for a given structure as a function of wide Isat compared to the change in Gm as a function of etch-stop position.

CONSIDERATION OF MMIC RESULTS

The bulk of analyses so far have focused on measurements of fundamental device behavior as a function of tweaks aim at improving intrinsic RF current swing and thus Psat. This section provides some illustrations of the impact of the variables considered on the performance of selected MMICs. This study involved the use of two important MMICs as test evaluation vehicles. Figure 7 shows the s21 response of the first MMIC as a function of etch-stop position and wide recess Isat. The standard etch stop position gives the best small signal gain.

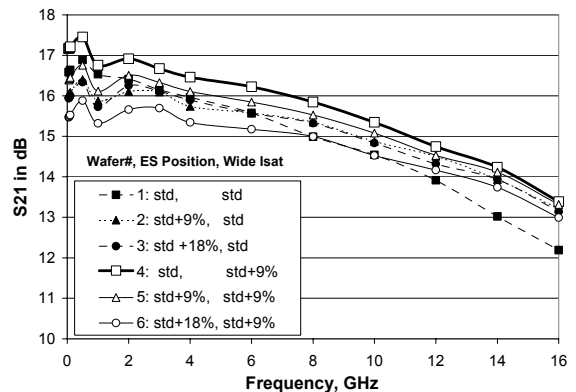


Figure 7: s21 of test MMIC #1 as a function of ES position and wide Isat.

The following trend chart illustrates that the improved process yields higher and more consistent output power, once the optimized process is implemented to improve the power performance of the devices

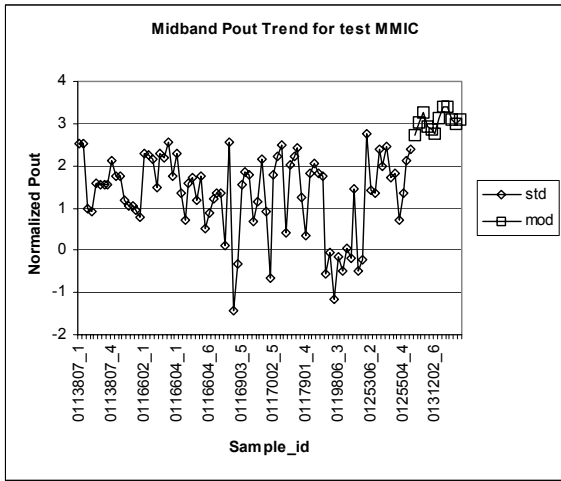


Figure 8: Midband Pout trend chart for higher power test MMIC (test MMIC #2)

PHYSICAL CONSIDERATIONS

Collectively, all of the DOEs considered addressed the impact of the following:

- Wide surface depth and the corresponding depletion depth as a function of surface treatment and material variables
- The condition of the ungated region of the gate recess channel.

It is interesting that the gate recess depth position does not show up

as an important factor among others considered. One should note, however, that the gate position of TriQuint's 0.50 um pHEMTs is set by an etch stop and that the presence of the Schottky sets a very consistent built-in potential. Ungated surfaces tend to have surface potentials that could vary significantly depending on the processing history of a given wafer. Moreover, depending on the wide recess current target, the resulting wide depletion edge position could easily extend beyond the depth of the gate contact. Thus, given the before mentioned points, it should not come as a surprise that the wide surface plays such an important role in establishing large signal performance characteristics.

CONCLUSIONS

The depth and prior history of the processing of the wide recess surface and the condition of the ungated gate recess surface play very important roles in establishing large signal FET characteristics. Careful preparation of the wide recess surface and positioning relative to the gate recess position can maximize instantaneous current swing and thus improve the intrinsic output power capability of a FET.

The co-planar FET cell approach allowed rapid feedback of process effects. Although the co-planar measurements were performed at low frequencies they were quite sufficient in diagnosing problems related to RF current swing.

REFERENCES

1. John B. Walker, " High Power GaAs FET Amplifiers", Artec House publications.
2. Ralph Williams, " Modern GaAs Processing Methods" Artec House Publishers
3. C.F. Campbell and S.A. Brown, " An analytical method to determine GaAs FET parasitic inductances and drain resistance under active bias conditions", IEEE Transaction on Microwave Theory and Techniques, Vol. 49. No7 July 2001.