Development of High-Gain and High-Efficiency InGaP/GaAs HBT for High-Voltage Operation

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Abstract

A high-gain and high-efficiency InGaP/GaAs HBT for high voltage operation has been developed. Saturated Pout of > 33dBm, peak PAE of > 70% and linear gain of > 22dB have been obtained for a 2 watt device at 0.9GHz and 2GHz. The device shows high burnout voltage at 10V operation and very high reliability for infrastructure applications.

INTRODUCTION

InGaP/GaAs HBT PAs are widely used in communication systems because of their high linearity and reliability. But most of their applications so far have been limited to low-voltage operation. Their high-voltage applications have been hampered by the breakdown voltage and thermal constraints. Several papers have reported good performance of high breakdown voltage (HBV) GaAs HBTs [1-3], but no reliability data at high-voltage operation has ever been reported.

This paper presents the development of HBV InGaP/GaAs HBTs with high-gain, high-efficiency and high-reliability for infrastructure (base station and cable TV) applications. Process capability and device reliability are also presented.

DEVICE FABRICATION

The HBT material structure includes InGaAs/GaAs emitter cap layer, InGaP emitter layer, C-doped GaAs base layer, n^- GaAs collector layer and n^+ GaAs subcollector layer. The devices were fabricated using a two-mesa structure, two-level metal interconnections with 5.5 µm plated Au as low-loss second level metal and heat spreader. Ion implantation was used for subcollector isolation. MIM capacitors with unit capacitance of 360 pF/mm^2, thin film resistors with sheet resistance of 50 Ohm/sq and through-wafer vias with 50 µm diameter were used for MMIC designs. Stack capacitors with unit capacitance of 660 pF/mm^2 are also available to reduce chip size. A 2W device with total emitter area of 1700 µm^2 was employed in this work to evaluate device performance.

Because of the thick collector layer, the base-collector mesa is higher than that of standard low voltage HBTs. To avoid interconnect metal step-coverage problem, a wet etch process was carefully developed to ensure a proper mesa sidewall slope. A set of process control monitor (PCM) patterns were designed and processed to monitor device performance and process parameters. Fig. 1 shows an array of first level metal (M1) going through several high base-collector mesas. The slope of the mesa was smooth which ensures M1 going up and down the mesas without breaks. Fig. 2 shows the SEM picture of a device after first level metallization.

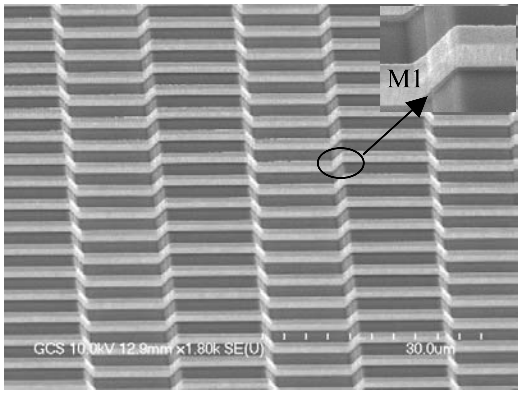

Fig. 1 SEM photo of first level metal going over base-collector mesa.

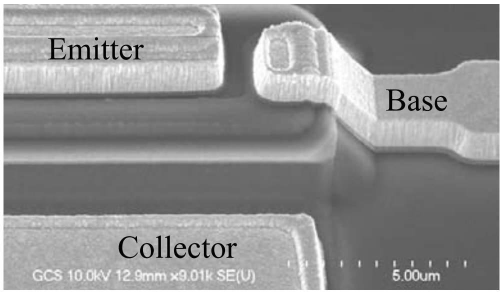

Fig. 2 SEM photo of device with 1.6 µm emitter width after first level metallization.

DESIGN CONSIDERATION

One major requirement for the HBV HBT development is a rugged device for high power operation. Several factors need to be considered: 1) optimal collector layer thickness and doping to meet breakdown voltage requirement, 2) proper layout design for thermal management, and 3) right ballast resistance value for thermal stability. The trade-off between these factors and device RF performance has been carefully investigated. The device burnout (or second breakdown) voltage at a certain collector current density (Jc) was used to evaluate device ruggedness. Although there is no simple correlation between device ruggedness at RF operation and DC burnout voltage, in general a higher burnout voltage makes the device more rugged. Fig. 3 shows the burnout voltage versus relative collector thickness for a 2W device at Jc of 5KA/cm^2. As expected, devices with thicker collector have high burnout voltages. However, too thick of collector will reduce the transistor's f_t and make the process more difficult. Fig. 4 shows the burnout voltage at Jc of 4KA/cm^2 versus relative ballast resistance value for a 2W device with a fixed collector thickness. Burnout voltage increases with increasing ballast resistance. The rate of increase tapers off after a certain value. Because the ballast resistor lowers the power gain, an optimal resistance value was selected to meet the device ruggedness requirement without significant power gain degradation. Through this trade-off study, we have established an HBV HBT design using the optimal epi structure, transistor layout, and a manufacturable fabrication process.

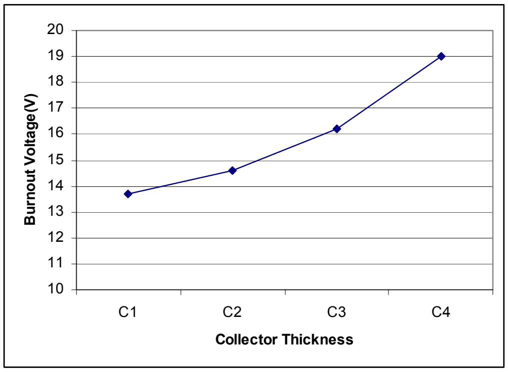

Fig. 3 Burn-out voltage vs relative collector thickness of a 2W device.

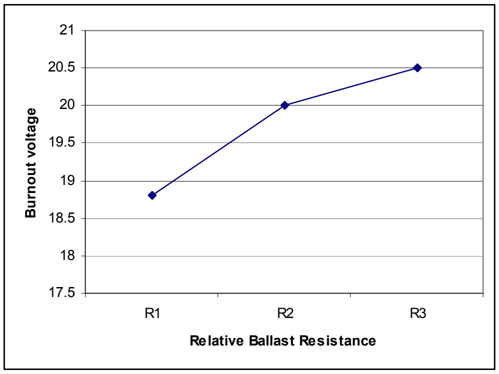

Fig. 4 Burn-out voltage vs relative ballast resistance of a 2W device.

DEVICE PERFORMANCE

The device has a typical current gain of 75, BVceo of 23V and BVcbo of 47V, which are suitable for nominal operation at 10 V. Fig. 5 shows the I-V curve of a 2W device. The device shows burnout voltage greater than 20V at Jc of up to 7 KA/cm^2. High current level is not shown in the curve due to current limitation of our test instrument.

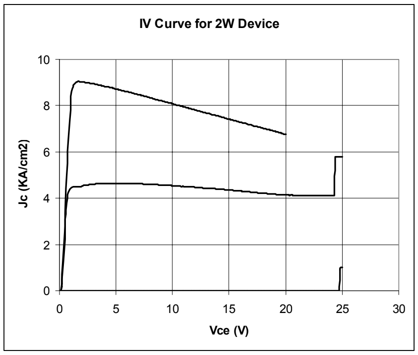

Fig. 5 I-V curve of a 2W device at current gain of 75.

The small-signal RF performance was tested on a device with emitter size of 1.6x30μm^2 at Vce of 3V. f_t and f_{max} versus Jc are shown in Fig. 6. Peak f_t and f_{max} of 40 GHz and 85 GHz are obtained, respectively. The onset of Kirk effect is at Jc of 30KA/cm^2. Even at Jc of 10KA/cm^2, the f_t and f_{max} values of 27GHz and 50GHz are high enough for 2GHz operation. The power performance of a 2W device was evaluated using a load-pull test system. At Vce of 10V and Jc of 10KA/cm^2, the device's power performance measured at 0.9GHz and 2GHz are shown in Fig. 7 (a) and (b) respectively. At 0.9GHz, 33.9dBm saturated Pout, 71.5% peak PAE, and 25dB linear gain were obtained. At 2GHz, the device measured 33.2dBm saturated Pout, 73% peak PAE, and 22dB linear gain. To our knowledge, this is the highest combination of gain and efficiency reported for InGaP/GaAs HBT at this power level.

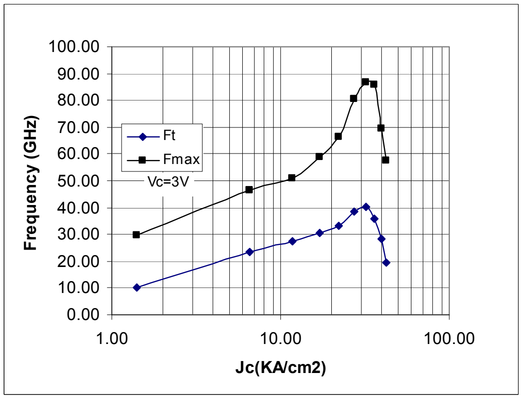

Fig. 6 f_t and f_{max} vs Jc for a device with emitter size of 1.6x30 μm^2.

PROCESS CAPABILITY

To evaluate the process capability, several PCM test patters were designed. One of them is a long chain of first-level metal connecting to emitter contact metal (M1-E chain). The M1-E chain consists of 88 pairs of interconnections as shown in the insert in Fig 8. This test pattern checks the quality of M1 to emitter metal contact, emitter metal to emitter contact, nitride via opening, and continuity of M1 on the base-collector mesa sidewall slope. Fig. 8 shows the SPC chart of the resistance of this M1-E test pattern. The Cpk is greater than 1.6.

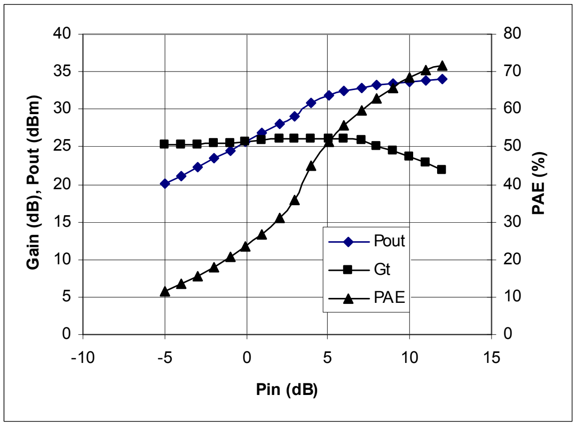

Fig. 7 (a) Power performance at 0.9 GHz. CW operation at Vce of 10V and Jc of 10KA/cm^2. Saturated Pout=33.9 dBm, Peak PAE=71.5% and Linear Gain =25dB.

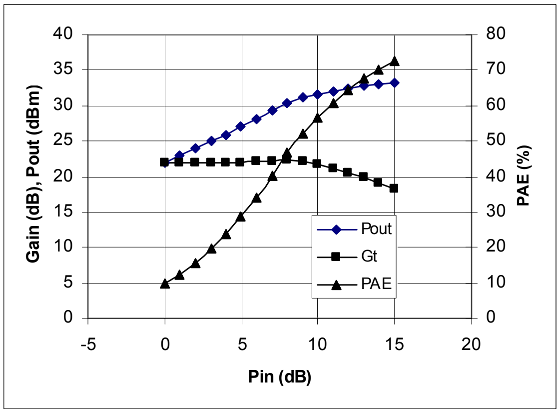

Fig. 7 (b) Power performance at 2 GHz. CW operation at Vce of 10V and Jc of 10KA/cm^2. Saturated Pout=33.2 dBm, Peak PAE=73% and Linear Gain=22dB.

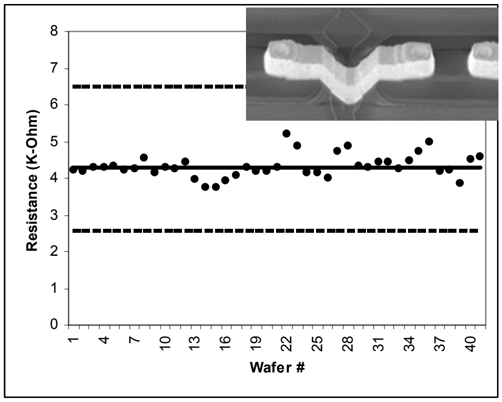

Fig. 8 SPC chart of M1-E chain resistance. Test pattern is shown in up-right insert.

A histogram of the HBT device's current gain from 50 wafers is shown in Fig. 9. The data was measured on PCM devices at 16 sites on each wafer. The average current gain was 74 with a standard deviation of 4.9. The Cpk was greater than 1.5. Fig. 10 shows the histogram of BVcbo with an average value of 47V and standard deviation of 2.5V. The Cpk is greater than 1. More than 16 PCM parameters were tested on each processed wafer. All 16 Cpk values were greater than 1. These data demonstrates that GCS' HBV HBT process has high performance and good manufacturability.

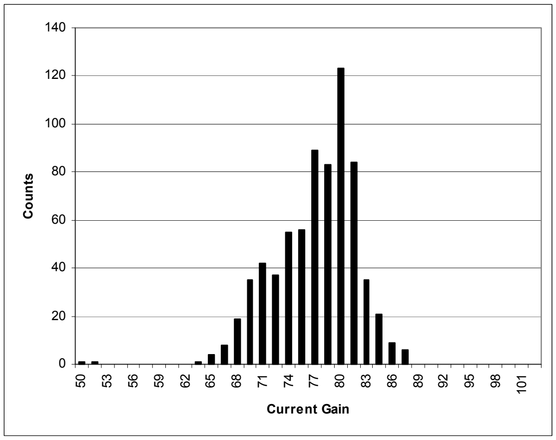

Fig. 9 Histogram of current gain from 50 wafers. Ave=74, Stdev=4.9, and Cpk > 1.5.

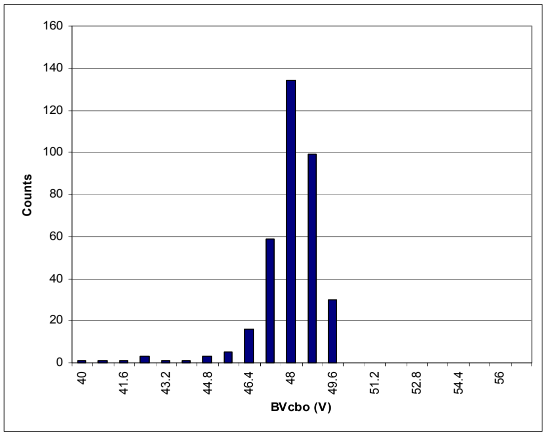

Fig. 10 Histogram of BVcbo from 50 wafers. Ave=47V, stdev=2.9V and Cpk > 1.

DEVICE RELIBILTIY

Three-temperature accelerated life tests of the HBV devices have been conducted at Tj's of 282°C, 264°C, and 238°C. These relatively low temperatures were selected to ensure that the dominant failure mechanism in these tests would be representative of the device failures at normal operating conditions. Devices were stressed at Vce of 10V and Jc of 15KA/cm^2. Fig. 11 shows the typical normalized current gain versus stress time plots at Tj of 264^{o}C. The failure criteria is defined as 40% current gain degradation from their initial values. The gradual degradation of current gain to about 80% is associated with the well-known hydrogen effect [4]. The continuous decrease after 80% may be due to high voltage bias [5]. The observed failure mode is a sudden gain drop, which is typical for InGaP/GaAs HBTs. An Ahrrenius plot is shown in Fig. 12. The projected MTTF of 7×10^6 hours at Tj of 125 °C, with activation energy of 1.1 eV, is sufficient to meet the stringent reliability requirement for infrastructure applications.

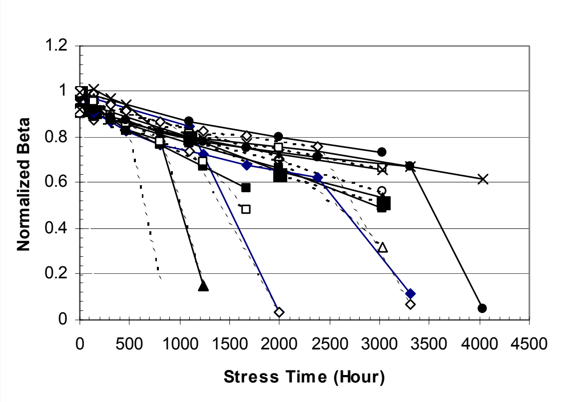

Fig. 11 Normalized current gain versus stress time at Vce of 10V, Jc of 15KA/cm^2 and Tj of 264°C.

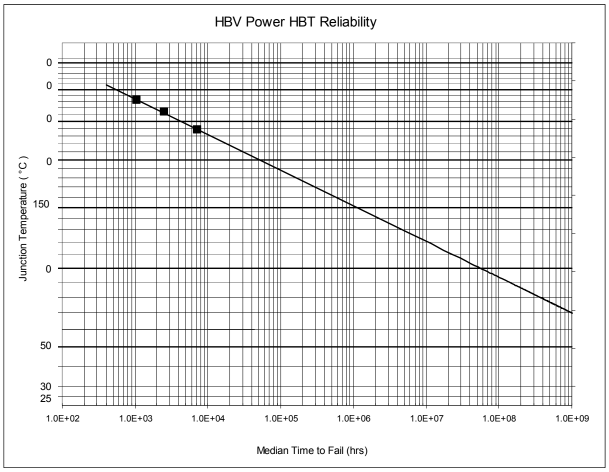

Fig. 12 Ahrrenius plot for HBV HBT process with activation energy of 1.1eV and projected MTTF of 7×10^6 hours at Tj of 125 °C,

CONCLUSIONS

In summary, we have developed a high-performance, high-reliability, and manufacturable HBV InGaP/GaAs HBT process for power amplifiers of up to 10V operation. This process is now offered for foundry services at GCS.

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RCRONYMS

HBT: Hetero-junction bipolar transistor
HBV: High breakdown voltage
MIM: Metal-isolation-metal
MMIC: Monolithic microwave integrated circuit
PA: Power amplifier
Pout : Output power
PAE: Power added efficiency
Tj: Junction temperature
MTTF: Medium time to failure
Jc: Collector current density