Building Solder Bumps on GaAs Flip Chip Schottky Devices

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Abstract

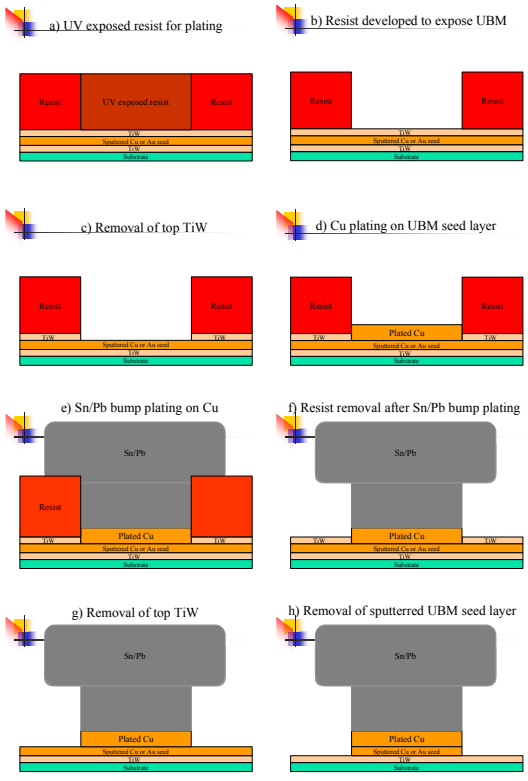
The semiconductor industry has made astonishing improvements in decreasing circuit dimensions and more importantly, greater performance. Making connections with gold contacts on GaAs devices using solder bumps instead of silver Epoxy offers lower contact resistance and hence, better performance. Further more, solder bump application to GaAs devices is amenable to high volume production and ease of manufacturing. Benefits from using solder bumps then become obvious for connections. This paper describes a process development using our existing technology of wafer processing in both wet and dry chemistries to build solder bumps on GaAs wafer for flip chip Schottky devices. Eutectic Sn/Pb solder bumps and Pb-free solder bumps were investigated. Detailed processing and chemistry will be discussed. Reliability of solder bumps on GaAs flip chip Schottky devices will also be presented.

INTRODUCTION

Microelectronic industry has been making a tremendous improvement toward miniaturization of circuitry with greater performance. Similarly the packaging and assembly of integrated circuits (IC) is aggressively making the effort to follow the microelectronic trend. Making connections with gold contacts on GaAs devices using solder bumps instead of silver Epoxy offers lower contact resistance and hence, better performance. Further more, solder bump application to GaAs devices is amenable to high volume production and ease of manufacturing, especially when circuit dimensions are getting smaller and smaller. Requirement of solder bumps for advanced packaging has created excitements among industries, especially equipment manufacturers, chemical suppliers and wafer fab. This presents not only a challenge to the industries but also a great opportunity for creativity and competitiveness. In fact, new consortiums like Semiconductor Equipment Consortium for Advanced Packaging (SECAP) and Advanced Packaging and Interconnect Alliance (APiA) have been formed recently to address these matters.[1] Many semiconductor companies, e.g., National Semiconductor, TI, Motorola, Fujitsu, Samsung, Hyundai and many others, are aggressively adapting and employing wafer-level chip scale packaging (WL-CSP) using solder bumps. To meet future's demand, the industry is constantly searching for both viable technique and more importantly, cost effective way to achieve its goal. All indications and predictions suggest that in order to meet future requirement, the packaging & connection for microelectronic industry has to adopt and employ solder bump technology. Comparing with stenciling and robotic ball placement, the electroplating technique is more cost effective for building solder bumps on wafers especially when ball pitch is much smaller.[2]

SOLDER BUMP PROCESS

In addition to many device fabrication processes, solder bump process requires photolithography and plating technologies. The entire solder bump process is described in the following schematic diagram in figure 1.



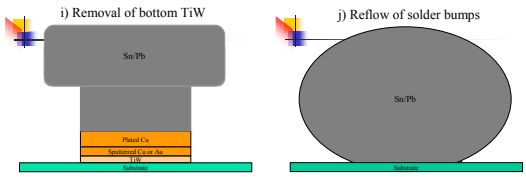


Figure 1. Schematic diagram of solder bump process.

UNDER BUMP METALLURGY (UBM)

A selection of appropriate under bump metallurgy (UMB) is critically important because it serves as a foundation on which the solder bump is built. There is a direct relationship between how good the UMB and the bump adhesion. Two types of UBM were experimented. One was TiW/Cu/TiW (1000 Aº/4000Aº/75Aº) and the other was TiW/Au/TiW (200 Aº/2250Aº/100Aº) as UBM for solder bump process. One set of wafers was sputtered with TiW/Cu/TiW (1000 Aº/4000Aº/75Aº) and the other set was sputtered with TiW/Au/TiW (200 Aº/2250Aº/100Aº). It has been tested that either type of UBM can be used as seed layer for plating.

PHOTOLITHOGRAPHY

Photolithography process is employed to create an exposed area on which solder bump is deposited using electroplating. G-line resist (465 nm) and I-line (365 nm) resist are commonly employed in the industry. Minimum resist thickness depends largely on the bump height. In general, the thicker the resist the better the control of a plating process and hence, the better uniformity of solder bumps. The following resists had been experimented, i.e., AZ4620 (Clariant), SPR220 (Shipley) and experimental resist 'TFP-V" (Clariant) which could impart 65 µm from single coating. All resists tested are acceptable for plating process. The SPR220 has been employed in our production line with 26 µm resist thickness.

PLATING PROCESS

Plating technology has been used for many years in other industries. Only recently, the microelectronics industry has realized the benefits and advantages of employing this technology. With combination of photolithography and plating processes, metal can be deposited selectively on wafers, resulting in desirable patterns of metal deposit. Accordingly, the plating technique is used to build solder bumps on wafers. The solder bump process requires two plating processes. Before plating can begin, exposed TiW (an adhesion promoter for resist) must be removed to expose copper or gold seed layer before copper plating. This can be accomplished by either a) wet etch using H_2O_2 or b) dry etch using SF_6.[3] These chemistries have been tested and they both are effective. Once TiW is removed, Cu plating is required to deposit 6 µm of Cu, often called copper post. Subsequently, eutectic Sn/Pb (either 63/37 or 5/95) plating or Pb-free solder bump plating is performed. The eutectic Sn/Pb plating chemicals from two manufacturers, i.e., Entone-OMI and Technic, had been experimented and proven to be equally good. Due to concerns of environment and alpha particle emission, the microelectronic industry is moving toward Pb-free solder bump (even though still many years away). The Pb-free solder plating had also been experimented using Shipley's Solderon BP TC 2000 (Sn/Cu: 98-99%/2-1%). The Pb-free solder bumps had been successfully demonstrated (see figures 3 and 5).

FIELD REMOVAL PROCESS

When solder plating and resist removal steps (using ST-23 from ATMI) are completed. It is necessary to remove field metal, i.e., either TiW/Cu/TiW or TiW/Au/TiW. We have many wet chemistries in house and been able to use in-house chemicals to remove the field metal. It is important that chemicals used for field metal removal will not attack GaAs surface. We have demonstrated that top TiW can be removed using either a) wet chemistry, e.g., H_2O_2 or b) dry etch, e.g., SF_6. Both Cu seed and Au seed can be removed using commercially available CN complexing chemical (for example from Technic). This chemical will react with Cu or Au and form $Cu(CN)_2^-$ or Au complex respectively.[4] Similarly, bottom TiW can be removed using same wet chemistry as the one used for top TiW removal. When all field metal is removed, the plated structure of bump looks like mushroom as shown in figure 2 for eutectic Sn/Pb (63/37) bump and figure 3 for Pb-free bump (Sn/Cu: 98-99%/2-1%).

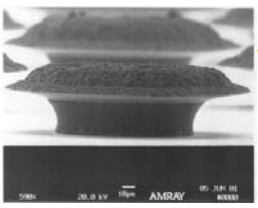


Figure 2. Before reflow.

Figure 3. Pb-free before reflow.

REFLOW OF SOLDER BUMPS

Eutectic temperatures of Sn/Pb (63/37), Sn/Pb (5/95), and Sn/Cu (99/1) are 183 °C, 314 °C and 227 °C respectively. Typically, a reflow temperature is higher than the eutectic temperature. In addition, an application of flux (e.g., RMA #5 from Indium Corporation) to the bumps before reflow step will promote nice formation of spherical bumps. Figure 4 shows results of Sn/Pn (63/37) after reflow @ 235 °C and figure 5 shows results of Sn/Cu (98-99%/2-1%) after reflow @ 245 °C.

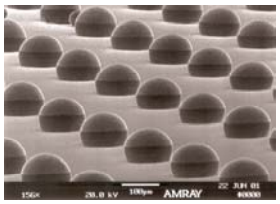


Figure 4. After reflow.

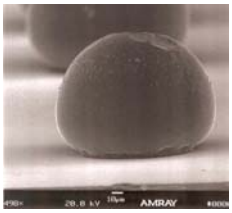


Figure 5. Pb-free bump.

It is postulated that flux not only prevents oxidation of Sn from Sn/Pb or Sn/Cu but also promotes a reduction of previously formed SnO and SnO_2 on bump surface resulting in nice hemispheric structures of the solder bumps as shown in figures 4 and 5. The flux can be removed easily using commercial resist stripping chemical, e.g., ST-23. Figures 6 and 7 show Sn/Pb (63/37) bumps on GaAs flip chip Schottky devices (GFCS4) before and after reflow respectively. Devices after reflow have been separated by dicing but still mounted on tape as shown in figure 7.

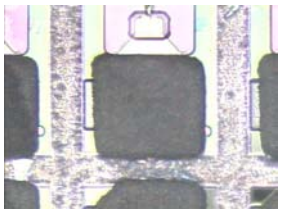


Figure 6. Before reflow.

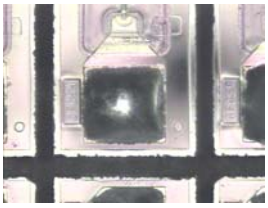


Figure 7. After reflow.

RELIABILITY

Having a solder bump process, GaAs wafer for flip chip Schottky devices was processed with solder bumps. After separation, flip chip Schottky devices were subjected to a reliability test using high temperature reverse bias (HTRB), 150 °C, 5 volts for 48 hr. Figures 8,9,10, and 11 show results of 52 devices before and after HTRB of forward voltage (Vf), breakdown voltage (Vb), total capacitance (Ct) and series resistance (Rs) respectively.

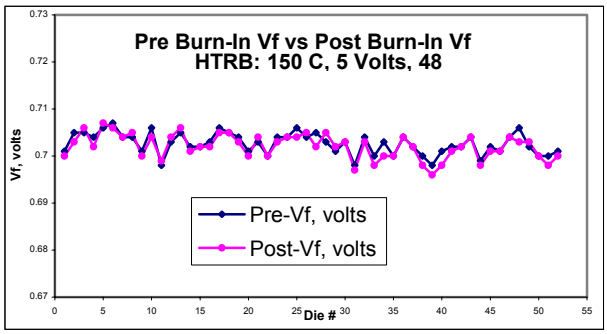


Figure 8. Vf before and after HTRB.

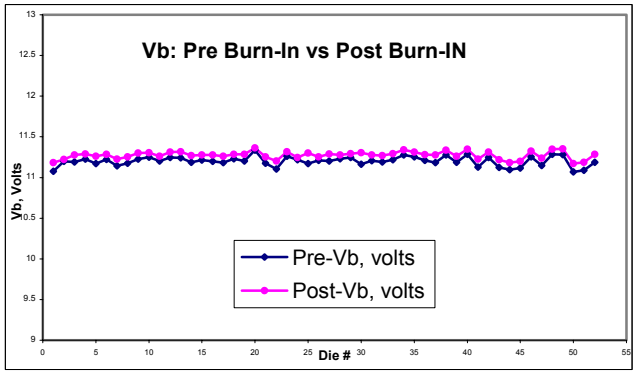


Figure 9. Vb before and after HTRB.

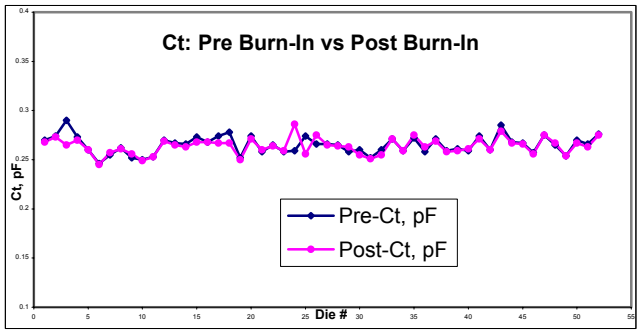


Figure 10. Ct before and after HTRB.

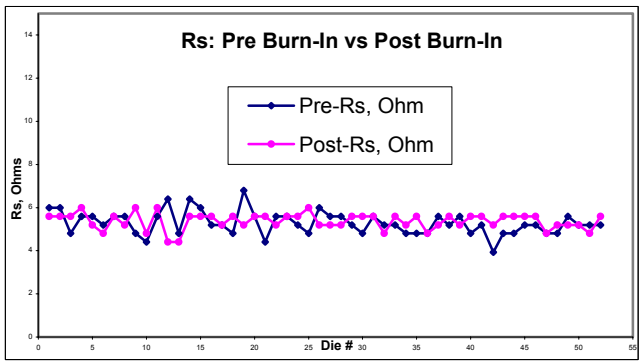


Figure 11. Rs before and after HTRB.

Preliminary results of the burn-in test certainly indicate that building of solder bumps on GaAs wafer for flip chip Schottky devices presents no reliability issue. Even though first phase of the burn-in period was only for 48 hr., an infant mortality failure, if it were to happen, would most likely occur during this initial period. These devices continue to be tested using HTRB for a long-term reliability study (i.e., 1000 hr.) and such burn-in test is still in progress.

BUMP SHEAR TEST

Bump shear test was conducted to test the adhesion and shear strength of the plated solder bumps using Dage 2400PC System and the test was performed according to the test method of JEDEC Standard No. B117.[5] For Sn/Pb(63/37) bumps with 48 µm height, 150 um in diameter, tip of probe from module surface was 7.62 µm with a shear rate of 127 µm/sec. For Sn/Pb(5/95) bumps with 11 µm height, 150 um in diameter, the tip of probe from module surface was 2.54 µm with a shear rate of 127 µm/sec. Bump shear tests were done at room temperature and an average of 20 measurements was taken. Shear strengths of Sn/Pb (63/37) and Sn/Pb (5/95) bumps were 85 gm/bump and 173 gm/bump respectively. These results indicate good shear strength from both types. Bases from which the bumps were sheared off exhibited intermetallic fracture of Sn/Pb material. This represents the failure mode # 1 which is an acceptable failure mode, according to JEDEC Standard No. B117.[5] Figures 12 shows results of the bases after the bumps of both Sn/Pb (5/95) and Sn/Pb (63/37) were sheared off.

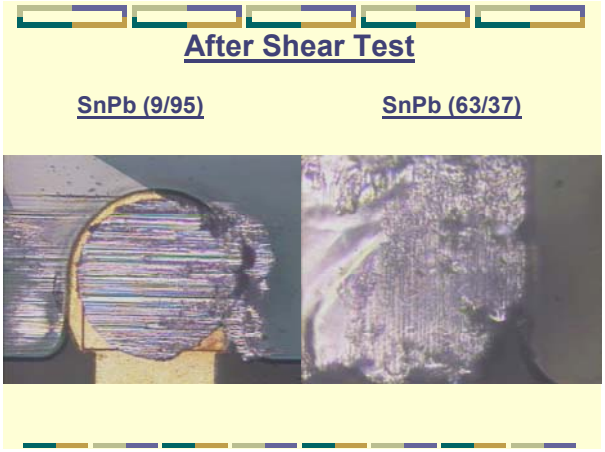


Figure 12. Results after shear test.

Even though devices with solder bumps have been successfully fabricated with good shear strength and tested reliably, an optimization of the entire process is still in progress. More importantly, the process must be capable of high volume production and compatible with packaging technique. This investigation merely represents a feasibility study and it is demonstrated that fabrication of solder bumps on small devices such as GaAs flip chip Schottky devices is possible.

CONCLUSION

We have successfully demonstrated an ability to build solder bumps (Sn/Pb and Pb-free) on devices. Several devices had been built with solder bumps. GaAs flip chip Schottky devices with solder bumps have been subjected to reliability test using high temperature reverse bias (HTRB). Preliminary results of HTRB show that devices suffer no adverse effect from the HTRB. Results of bump shear tests indicate strong shear strength of both Sn/Pb (63/37) and Sn/Pb (5/95) bumps. This study has demonstrated that construction of solder bumps on GaAs flip chip Schottky devices is possible. Solder bumps can potentially be incorporated as a part of interconnection for high performance devices. Despite a success of building solder bumps on devices, we are certainly not in a position for a large volume production. New equipments like a thick resist coating track and more importantly, automated wafer plating equipment are required. Further, the devices with solder bumps must be compatible with existing packaging technique.

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