High Yield Lithography and Wafer Handling Methods for Reliable Backside Processing of Brittle III-V Materials

C. Schaefer[1], V. Dragoi[1], S. Farrens[2], M. Wimplinger[1], P. Lindner[1]

[1]EV Group E. Thallner GmbH, DI Erich Thallner Straße 1, A-4780 Schärding, Austria
[2]EV Group Inc., 3701 E. University Drive, Suite 300, Phoenix, AZ 85034, USA
E-mail: C.Schaefer@EVGroup.at, Phone: +43 7712 5311-0

Keywords: thinned III-Vmaterials, automated backside lithography, automated temporary bonding and de-bonding

Abstract

This paper focuses on state-of-the-art backside lithography technology for advanced applications in compound semiconductor material processing. The need for thinned III-V materials with a thickness below 100 or even less than 50 micron in high frequency as well as power devices creates new challenges in the handling of those extremely fragile and costly substrates. Breakage of such brittle substrates during manufacturing can create significant expenses for high volume manufacturers. The risk of damage is increased also by the multiple processing steps required, and again when using backside processing for vias generation.
This paper describes solutions for automated backside lithography processing in terms of handling and pre-alignment as well as the reliable preparation of those materials prior to the backside processing sequence via automated temporary bonding/debonding technologies using a dry adhesive thermal release film. Furthermore recent results on alignment accuracy during the backside lithography will be presented and the TTVs achieved by different temporarily bonded material combinations.

INTRODUCTION

In recent years, several technologies have been developed for the production of portable, mobile systems such as handheld computers, phones etc. All these applications have one requirement in common: low power consumption for long-term remote operation. Thus, microelectronic devices have to operate more efficiently and typically at higher frequencies in order to meet these requirements.

One idea on how to overcome this challenge is to reduce losses and parasitic effects within the devices. The main approach used to achieve this is to thin the substrate material itself, as only the top layer is required for electrical functionality. The bulk of the material is used for mechanical stability during processing and causes reduced operational performance.

Thinning the substrate material is the most logical way to resolve this problem but can have a major drawback in terms of yield risk. Breakage of the processed and brittle substrates can create significant expenses for the manufacturer. Compound materials like GaAs, InP, SiC and others are expensive as basic materials and their value increases dramatically during processing; several thousands of dollars per substrate is not an uncommon value.

RELIABLE HANDLING ON CARRIER VIA FULLY AUTOMATED TEMPORARY BONDING AND DEBONDING

Handling of those delicate III-V materials is carried out by means of temporarily "gluing" (= bonding) the substrate to a rigid carrier (see Fig. 1). The use of a carrier substrate improves the mechanical strength while an intermediate layer (heat- or UV-release adhesive film or wax) reliably bonds and further protects the active surface of the device wafer during grinding, polishing and subsequent backside lithography processes[1]. This type of bonding is termed temporary because device and carrier substrates can be debonded once back thinning and backside lithography have been completed. Quartz and sapphire are common carrier materials for this purpose, as they are both rigid and transparent, allowing access for optical alignment during wafer processing.

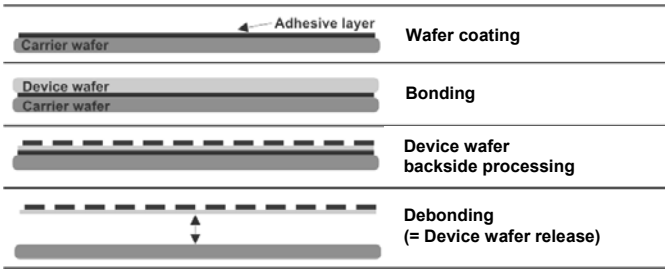

Fig. 1: Process flow for brittle wafers handling using temporary wafer bonding and debonding.

Fig. 2 shows a typical automated process sequence executed in a fully automated production bonding equipment. The dry and double side adhesive film is applied to the III-V wafer device surface prior to the start of such a process sequence.

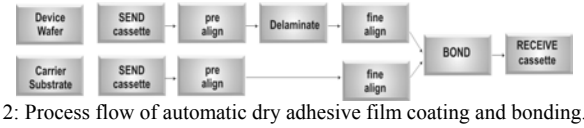

Fig. 2: Process flow of automatic dry adhesive film coating and bonding.

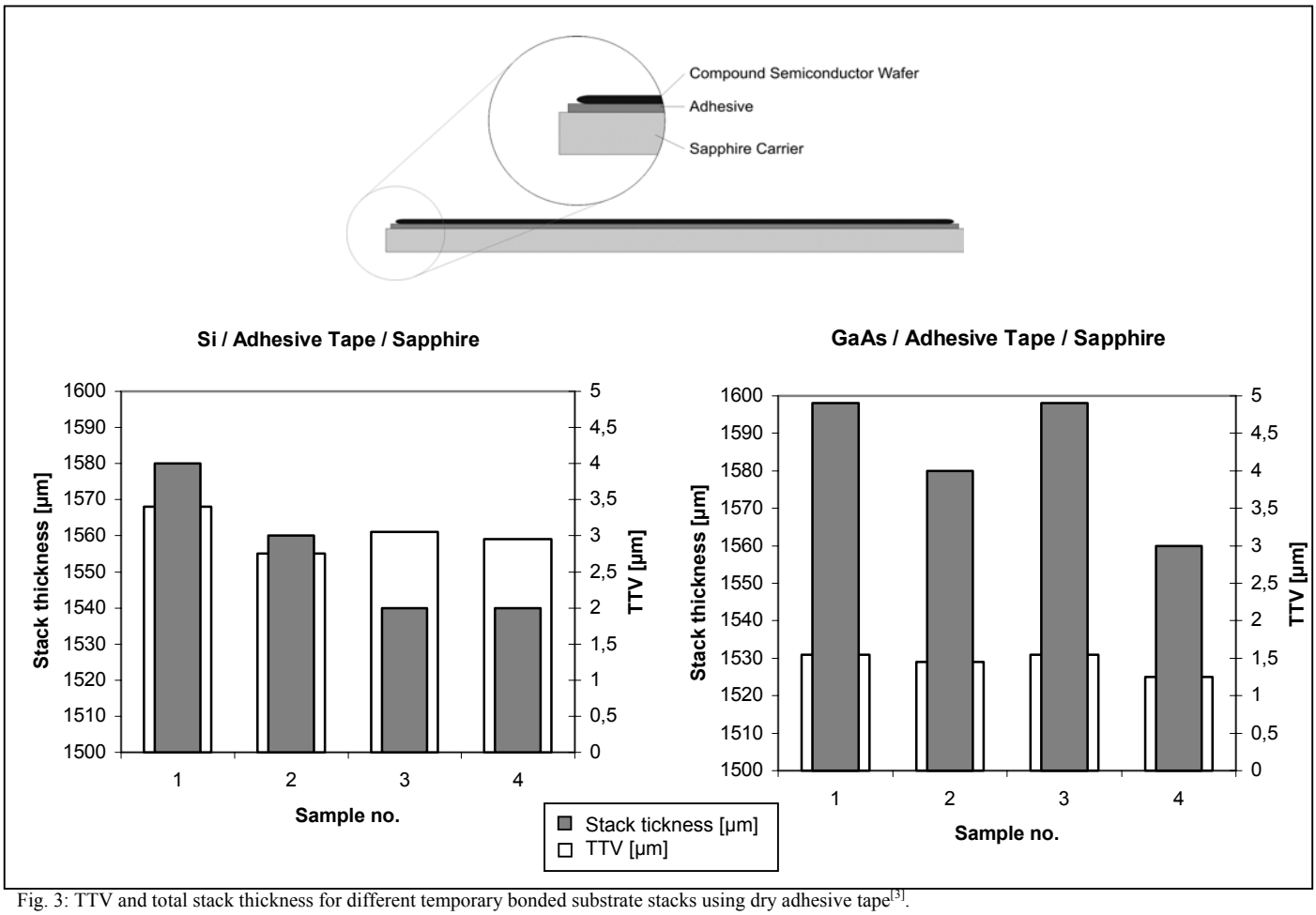

Fig. 3: TTV and total stack thickness for different temporary bonded substrate stacks using dry adhesive tape[3].

Of crucial importance to the temporary bonding step is uniform pressure across the entire surface area. This is required in order to achieve low TTVs for the bonded substrate stack. Using dry film adhesive intermediate layers and fully automated processing, the achievable TTV of a GaAs wafer (150 mm, 675 micron thick)/dry film/sapphire (153 mm, 700 micron thick) stack is between 2 to 5 microns (see Fig. 3).

The debonding process is schematically shown in Fig. 4.

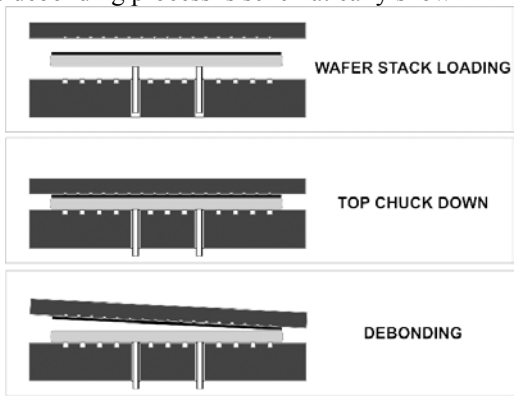

Fig. 4: Debonding procedure for Revalpha dry film adhesive reversible bonding.

The wafers are automatically loaded into the process chamber. Three retractable loading pins allow the robot arm to perform this operation. The wafer stack is brought into contact with the bottom chuck (carrier wafer on chuck), and then the top chuck is brought into contact with the device wafer. Both chucks have vacuum grooves for wafer sustaining and can be independently heated.

The wafer stack is heated up to the release temperature of the Revalpha film and then the top chuck is gently tilted in order to start the wafers debonding from the wafer rim. This also decreases the probability of the device wafer shattering due to the mechanical stress, which can occur during debonding due to the sticking effect[3].

BACKSIDE LITHOGRAPHY CHALLENGES

Depending on the type of process, the new substrate (III-V wafer bonded to sapphire) may need to be pre-aligned, e.g. for spin coating. The current technology of mechanical or optical pre-aligners (see Fig. 5) will accommodate this easily under the following necessary precondition: the bonding process has to be performed properly so that no adhesive material (like adhesive, wax, polyimides, etc.) is protruding

from the device substrate edge. Otherwise pre-alignment cannot be executed with the required precision.

In terms of the exposure of substrates, there are additional challenges to overcome. The typical pre-alignment is based on the outer edge of the whole substrate. This is suitable in terms of centering for a spinning process but not accurate enough for an exposure process. As the device wafer and carrier are not ideally centered - typically +/- several 100 µm are achievable - a mechanical pre-alignment will not automatically provide an acceptable pre-alignment. The fine alignment typically performed with pattern recognition systems takes much longer as bigger search areas need to be defined and scanned in a limited field of view through standard magnification optics.

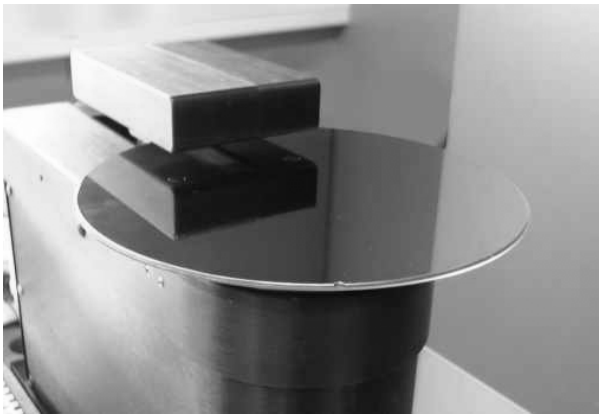

Fig. 5: Pre-alignment of III-V wafer and sapphire carrier.

The ideal solution is to pre-align in reference to the device substrate. EVG refined the use of a standard optical pre-aligner to accommodate the recognition of any material edge, whether it is Si, GaAs, glass, quartz or sapphire. A regular CCD-line scan chip enables safe and accurate detection of all these materials.

The challenge is in making this setup sensitive to several edges caused by different materials on one substrate. This was solved by means of modifying the wavelength of the appropriate light source. By also utilizing a software algorithm, the first edge of the transparent carrier as well as the second edge of any other material is detected accurately. Thus, a proper centering of wafers in reference to the device substrate can be achieved, providing proper positioning for the alignment and exposure steps. With the minimized search area, the pattern recognition completes its job in a shorter timeframe and within the performance specs.

Another challenge in the lithographic processing of temporarily bonded substrates occurs when backside processing is needed. Applications may require a backside lithography process for etching vias, enabling direct packaging approaches or for interconnections[2].

In this case, the substrate is bonded with the active surface towards the transparent carrier. The backside alignment procedure uses a state-of-the-art bottom side splitfield microscope incorporating position data storage by means of crosshair or image overlay. This positioning must be performed through the carrier material. However, even transparent quartz or sapphire material will cause a shift in focus towards the device surface.

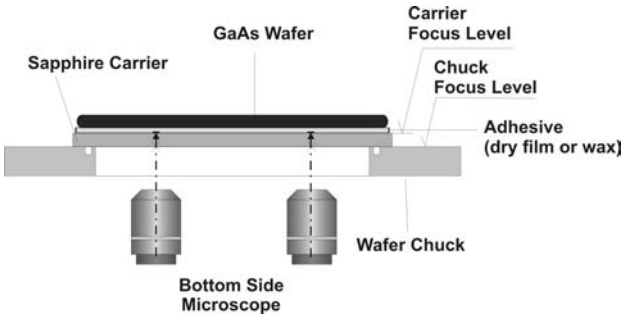

Fig. 6: Principle of backside alignment with sapphire carrier.

Usually, refocusing results in a certain amount of shift and misalignment. When the required alignment accuracy is very precise (+/- 1 µm), this can easily result in an out-of-spec product.

The unique Z-movement mechanism in EV Group's EVG®620 series mask aligners allows a different approach. As in the backside alignment procedure, the Z-movement is performed by the mask, and not via spindles as in conventional systems. With this patent pending design, refocusing can be avoided for carrier-based alignment as well. Using a blank carrier and referencing the mask, the fixed microscope position can be maintained even in this application and provide accurate results similar to regular backside applications.

CONCLUSIONS

Using proven equipment technology with some modifications for temporary bonding and debonding as well as for backside lithography, the problems of high-risk processing on III-V semiconductors can be overcome and efficient yield with these costly materials can be achieved.

REFERENCES

[1] C. Schaefer, T. Glinsner, T. Luxbacher, P. Lindner, R. Michaels, J. Palensky, V. Dragoi, M. Reiche; *Reversible and Permanent Wafer Bonding for GaAs Processing*, Proceedings of 2001 GaAs MANTECH - International Conference on Compound Semiconductor Manufacturing Technology, May 21-24, 2001, Las Vegas, p. 192-195

[2] P. Lindner, C. Brubaker, T. Glinsner, C. Schaefer, M. Tischler, *3D Interconnect through Wafer Level Bonding*, presented at SEMI Technical Symposium, Semicon Taiwan, September 16-19, 2001 Taipei, IC Seminar III

[3] V. Dragoi, T. Glinsner, G. Mittendorfer, M. Wimplinger, P. Lindner, *Reversible wafer bonding for reliable compound semiconductor processing*, IEEE Proceedings 02TH8618, volume 2, CAS 2002, Sinaia, Romania, pp 331-334

