Advanced Commercial InP HBT IC Process

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ABSTRACT

An advanced, high-performance 4-inch InP HBT process technology has been offered for commercial pure-play foundry services by GCS for the last two years. In this paper, we reported on recent advances of our proprietary device design and process technology, GCS's InP HBTs show potentially excellent reliability under lifetests at current densities of 100kA/cm^2 and higher. State-of –the-art circuit performances have been demonstrated by our customers designing into our baseline InP HBT process technology; which we believed are strong evidences of the readiness of InP HBT technology for mainstream IC production.

INTRODUCTION

Indium Phosphide based process technology represents a disruptive technology platform because it can be used to build both ultra-fast electronics as well as photonics integrated circuits; thereby truly integrate the manipulation of both electrical and optical signals in a single chip. In particular, InP-based HBT is ideally suited for all high speed and low power digital-analog applications, militarily and commercially [1-6]. However, access to InP-based process technology has been very limited. Traditionally, it has been confined to the exclusive domain of a few large defense companies with sizable R&D investment and captive fabs; thus restricting its utilization in mainstream IC industry. In recent years, the availability of commercial foundry service for state-of the-art InP-based HBTs has enabled much wider accessibility of this high performance process technology to all IC designers.

As a pure-play foundry, GCS has been offering an InP baseline process with 1μm minimum emitter width for both SHBT and DHBT. The devices performance (SHBT – f_T& F_{max} >170GHz; BV_{ceo} > 3.5V; DHBT – f_T& F_{max} >160GHz, BV_{ceo} > 8V) has satisfied very stringent demands required for optical networking PMD circuits and applications [7]. Many customers have designed into our InP HBT baseline process, and was successful in demonstrating state-of-the-arts circuit performance. These results provide strong testimonies to the conjecture that InP HBT is making a solid entrance into mainstream commercial IC applications.

BASELINE FABRICATTION PROCESS

GCS 4-inch InP HBT baseline process lots are ran in the same line as that of our production-ready GaAs-based 4-inch HBT line; thereby leverage process modules (photolithography, thin film, etch etc.) maturity and controllability. Key features of GCS's InP HBT process are: mesa-etched isolation and planarized process using a low permittivity dielectric; low-loss multiple levels interconnect; and high yield, non-self aligned devices with minimum emitter width of 1μm. The industry-standard I-line production stepper has been employed to define all photolithography steps.

Device reliability concern has been integrated to our InP HBT baseline process development from the very beginning. Starting from the epitaxial structures to the fabrication processes, awareness of potential reliability issues has been paid close attention to. An Al-free InP emitter (instead of AlInAs emitters) and carbon-doped base (instead of the commonly used Be) have been employed in the device epi-structure to improve reliability. A non-alloyed Ohmic metal contact scheme has been developed to enhance the robustness of the devices under high current drive. A proprietary passivation technology was applied to ensure surface cleanliness and enhance reliability for our InP HBT technology.

DEVICE CHARACTERISTICS AND MODELS

Fundamental to our ability to offer foundry service for InP HBT process technology is the robustness of the device characteristics and models. Thorough and systematic characterization of our devices has enabled us to develop an excellent compact VBIC model for InP HBT devices. Shown in Figure 1 are plots of common-emitter current-voltage characteristic at 25C and 125C for a nominal 1x3 μm^2 InP SHBT, along with the large-signal VBIC model of the device. As can be seen, the model shows excellent fit to the measured data over the entire range of nominal operating voltage and current density from 25C to 125C. Device self-heating and impact ionization effects are built into the model and can be seen to account for the device behaviors at high current and high voltage.

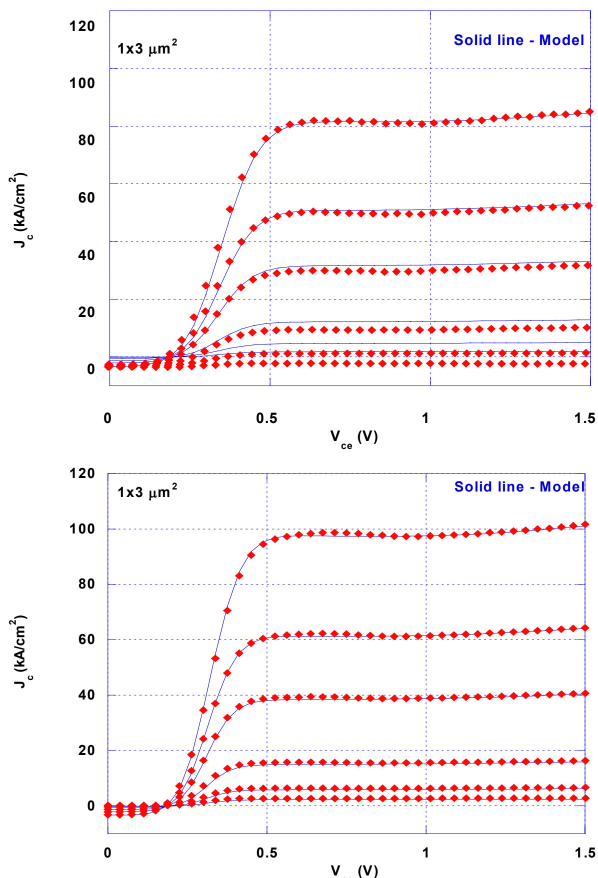

Figure 1: Common-emitter characteristics of a baseline InP SHBT with 1x3 μm² emitter: Top – 25C, Bottom – 125C (Points are from the measurements and solid lines are from VBIC model).

Cut-off frequency (F_t) of over 200 GHz has been extrapolated from RF characterization on these devices at an emitter current density of 160 kA/cm². Shown in Figure 2 is the plot of F_t versus current density at various collector-emitter bias voltages for the device. Again, excellent fit is observed between measurement and model throughout the biasing conditions.

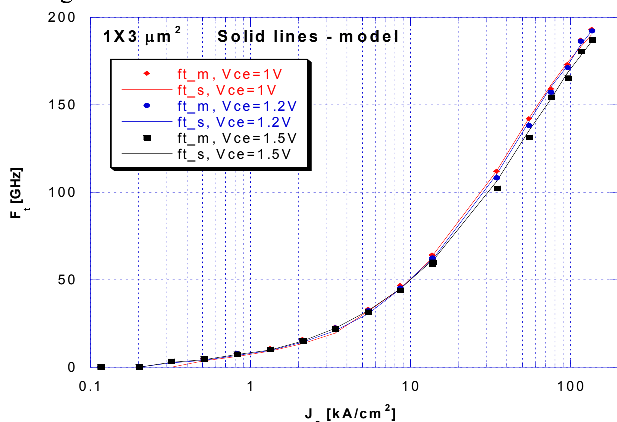

Figure 2: F_t versus current density at various collector-emitter voltages (Points are from actual measurements and solid lines are from the model)

DEVICE RELIABILITY UNDER LIFE-TEST

Systematic characterization of the reliability of our InP HBTs, have started early on in the process development. InP single junction bipolar transistors (SHBTs) with emitter size of 1x3μm² were subjected to accelerated life-test at multiple junction temperatures (T_j) and multi-current density (J_e) from 100kA/cm² to 150kA/cm². The stressed devices were cooled to room temperature and DC characterized using HP parameter analyzer 4155B. The tracked parameters include: (i) *Beta*, DC current gain measured at I_c=3mA (or 100kA/cm²); (ii) V_{be}'s, Base-Emitter voltages, corresponding to I_c=1μA and 3mA, on Gummel plots; (iii) R_e, emitter resistance.

Figure 3 shows the beta degradation for ten devices as a function of stress time for the T_j=210°C with J_e=100kA/cm². The DC gain (Beta) shows stable characteristics up to 8000 stress hours.

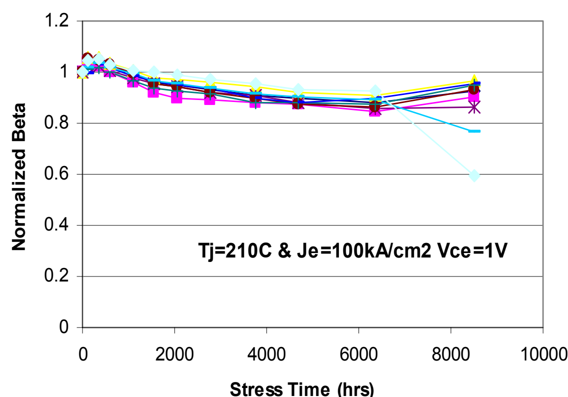

Figure 3: Normalized Beta degradation over stress time for T_j=210°C and J_e=100kA/cm².

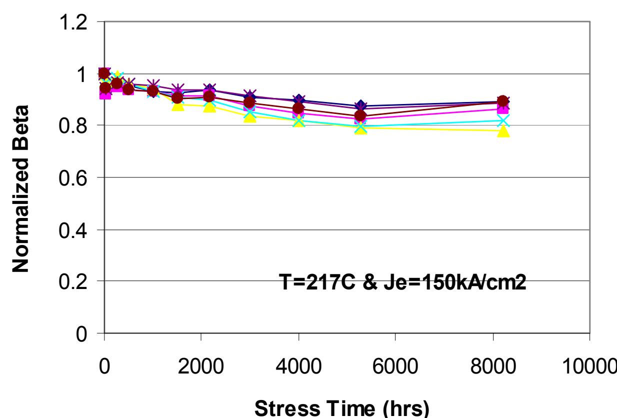

Figure 4: Normalized Beta degradation over stress time for T_j=217°C and J_e=150kA/cm².

Test at higher current density are also carried out. Figure 4 shows the beta degradation over stress time for

J_e=150kA/cm^2 and T_j=217°C. Device stability is also observed for over 8000 hours of testing. The third group with J_e=150kA/cm^2, and higher junction temperature, T_j=252°C, was also carried out (Figure 5). Again, the DC gain is also observed to be stable for over 4000 hours under 150kA/cm^2 current density stressing. From the beta degradation data, most stressed devices show less than 20% degradation and tended to be stabilized for period of time. We have not observed the sudden beta drop failure mode, which is commonly found in GaAs based HBTs yet.

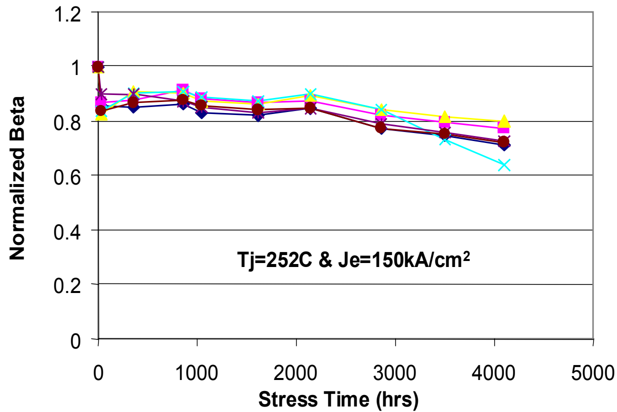

Figure 5: Normalized Beta degradation over stress time for T_j=252°C and J_e=150kA/cm^2.

All the stress tests are still on going. We have not specified a failure criterion yet until more data are gathered such that we can capture the true failure mode and extract the activation energy. Comparing to reported data, the stress conditions that we have subjected our HBTs to are much higher, therefore we expect the lifetime under similar stress conditions as those reported, the lifetime should be much higher on our SHBT. The reported activation energy for InP HBTs is range from 1.0eV to 1.8eV [4-6]. A simple estimation is applied to our InP HBTs by using activation energy E_a=1.0eV and current acceleration factor, n=1.0, and the estimated MTTF at junction temperature Tj=125°C is greater than 10^7 hours [9].

CIRCUITS PERFORMANCE USING GCS InP HBT

Utilizing GCS InP SHBT foundry process, record-setting circuits have been published. These results provide strong testimonies to the readiness of InP HBT entrance into commercial IC production. Furthermore, they asserted that InP HBT is the device technology of choice for high performance applications. First pass success with state-of-the-arts circuits have been reported (Figure 6&7). Recently, a ring oscillator with record low gate delay of ~2 ps was demonstrated (Figure 8).

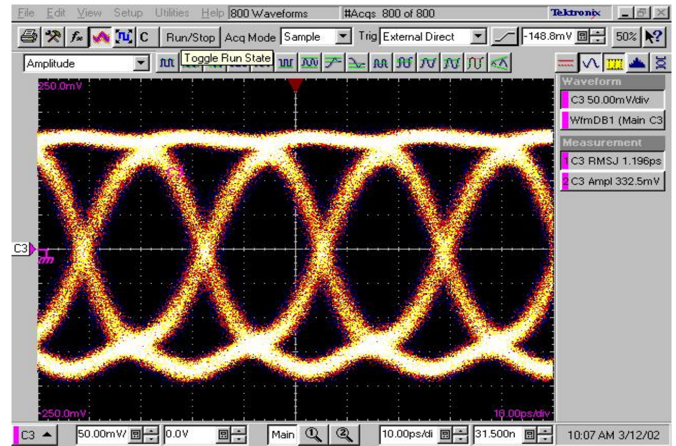

Figure 6: Measured eye diagram of a 43 Gbps MUX circuits using GCS InP SHBTs. (Courtesy of Inphi Corporation).

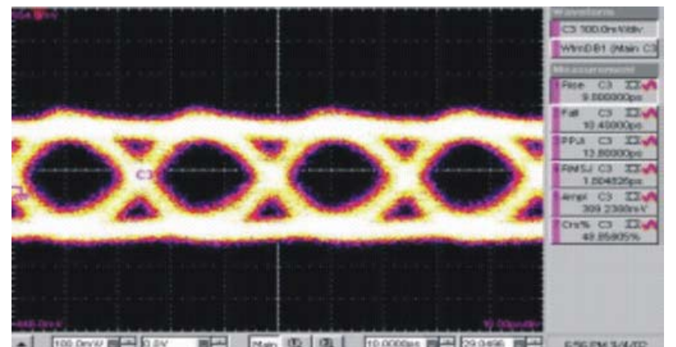

Figure 7: Eye diagram of a TIA circuits with bandwidth greater than 40 Gbps. (Courtesy of Inphi Corporation)

Recently, a 17 stages ring oscillator (13.2mW/stage) with record low gate delay of ~2 ps was also demonstrated (Figure 8) [9]. This is the lowest gate delay reported for all semiconductor technologies.

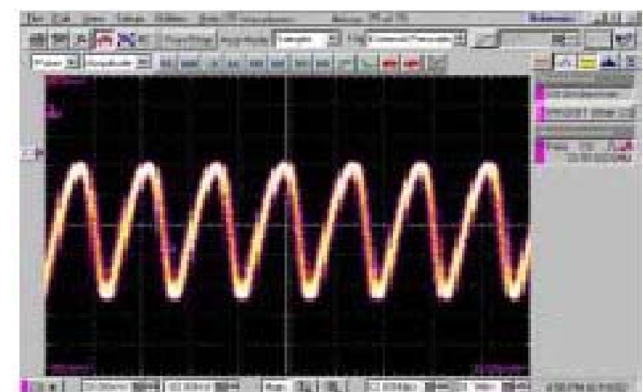

Figure 8: Oscilloscope eye diagram of output voltage waveform of a 17 stages InP SHBT ring oscillator circuits under normal mode of oscillation. (Courtesy of Inphi Corporation)

Other high performance circuit topologies have also been designed using GCS InP HBTs. Shown in Figure 9 is a tunable common-base TIA circuits performance, featuring among the highest Tz-BW/Pdc ratios for 40G TIAs [10].

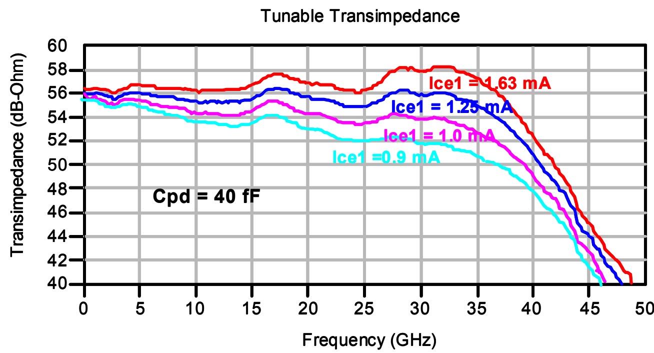

Figure 9: Measured transimpedance response for various CB tuning bias currents: Ice1=0.9, 1.0, 1.25, 1.63 mA (Courtesy of Sirenza Microdevices)

CONCLUSIONS

An advanced commercial InP HBT process technology has been established at GCS. Excellent agreements between device characteristics and compact device models have been demonstrated, which enable designers to design and simulate high performance circuits. On-going HTOL testing yielded stable device characteristics after >8000 hours of stress testing. A conservative estimation (E_a= 1.0 eV) of MTTF at junction temperature Tj=125°C is greater than 10^7 hours, which would satisfy the stringent requirement of most commercial applications. Record setting circuit performance demonstrated by different customers demonstrated that the device technology is ready for mainstream commercial entrance.

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ACRONYMS

InP: Indium Phosphide
SHBT: Single Heterostructure Bipolar Transistor
DHBT: Double Heterostructure Bipolar Transistor
HTOL: High Temperature Over Life