High Power Ka – Band PIN Diode Technology

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Abstract

A PIN diode process is described with over 70 volts breakdown voltage and a series resistance of 1.3 Ω. The integrated process includes thin film resistors that enable the design and realization of Ka-Band, non-reflective high power switches with on-chip terminations.

An advanced top metal lithography is used with critical dimensions of a few microns for the implementation of fine elements such as Lange couplers, over a very aggressive topography of 6.5 μm.

The process flow enables both micro – strip and co-planar (CPW) designs.

S parameters of shunt micro-strip diodes were measured from 0 to 50 GHz. Insertion loss for the reverse biased shunt-diode were 0.2-0.4 dB and isolation over 24 dB at 20 mA forward bias (Fig. 4,5).

The diodes were RF and DC tested at elevated temperatures, under high current stress. The results of the reliability tests are discussed.

INTRODUCTION

PIN diode has been known for many years now as the best device for high power switching applications due to the high breakdown voltage and low on-state series resistance. However, only a few foundries really managed to manufacture a state of the art device that has a breakdown voltage as high as 70 volts and a series resistance of 1.3 Ω.

In the technology described, TaN thin film resistors (TFR) are integrated in the process flow, in addition to the traditional High Power PIN based MMIC technologies [1,2]. The TFR enables the design and realization of Ka-Band, non-reflective high power switches with on-chip terminations (Figure 1).

The purpose of the paper is to describe the development of the PIN diode fabrication process. A number of isolation approaches between different circuit elements have been evaluated; among them, various epitaxial buffer layers and dielectric film. The diode is characterized by DC and RF electrical testing. Reverse breakdown voltage is measured at 10μA and S parameters are measured at forward bias of 20 mA and Reverse bias of –5 volts. The diode series resistance is also monitored from the S-parameters measurement.

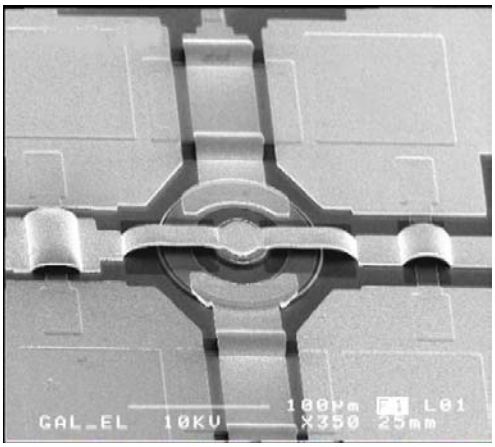

Figure 1–CPW diode, SEM inspection.

PROCESS

The circuit designs implement shunt diodes, Air-bridges connecting the anode to the transmission lines and the rest of the circuit elements (Figure 2,3). The Air-Bridge is designed to the maximum possible width to enable the maximum current handling capability. Wet etching is used to perform the diode mesa structure. Via holes connect the cathode contact to the backside ground of the micro-strip transmission lines. The cathode can be easily connected also to the ground lines of a Co-Planar Wave-guide (CPW) transmission line. The anode contact is formed from Pt\Ti\Pt\Au stack. The Pt as the base layer performs a good contact to the GaAs and reduces the anode contact resistance.

Silicon Nitride has been applied as the MIM capacitors dielectric layer and the diode passivation layer. The silicon Nitride layer forms capacitors with a breakdown voltage higher than 100 volts.

TFR are formed on top of the Silicon Nitride. The Sheet resistance was chosen to be 50 ohms per square to enable a relatively high maximal current capability. The Resistors are patterned over the high topography by Lift-Off techniques

that use LOR as the base layer for the Photoresist. The lithography process reached a very good uniformity and a tight CD control.

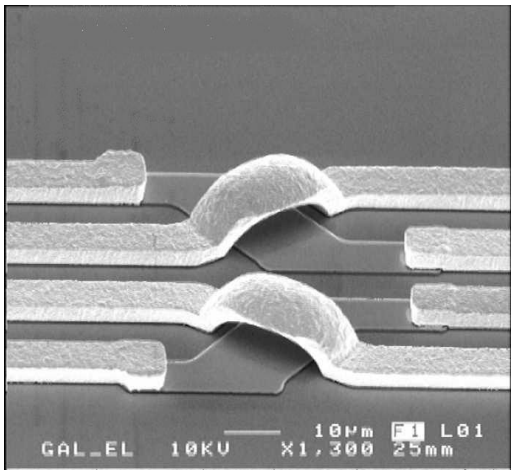

Figure 2-couplers, SEM inspection.

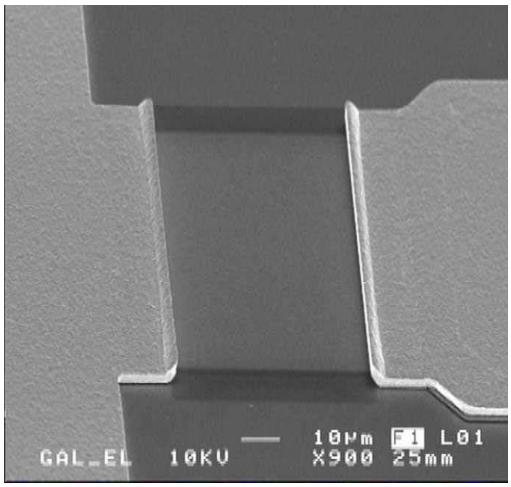

Figure 3-TaN resistor, SEM inspection

The major technological challenge was the definition of MMIC elements with tight CD over a very aggressive topography of over 6.5 µm. Under these conditions the Air-Bridge layer was one of the most challenging tasks. In this layer we define the crossovers, but also Lange couplers, capacitor top electrodes, and other elements that are sensitive to line width variation. Air-Bridge metal definition is based on electro-plating technique. The bottom photoresist layer was restricted to the places where elevated line is needed, known as "Open-Via". The technological challenge was thermal stabilization of the very thick bottom photoresist layer, to survive the top photoresist definition. Two different approaches where tested. One approach was doing a post exposure bake (PEB) at a high temperature, with no hard bake. This approach gave steep photoresist profile (square profile of the bridge), with good thermal stability. The drawback of this approach was the narrow process window, which varied between lots, causing, in some cases, bubbles in the photoresist during PEB. The second approach was to use standard soft-bake, no PEB and elevated hard-bake. This in turn caused a flow of photoresist during hard-bake, resulting rounded bridge profile. The second approach was chosen due to the wider process window and the higher mechanical strength of the rounded bridges.

Since most of the designs are for high power applications, the isolation between different elements of the circuits, mainly the bonding pads, is a very important issue. A choice of the appropriate buffer layer and the correct pad layers, improves dramatically the isolation between bonding pads at temperatures up to 130 °C. That is well above most relevant circuits working conditions. When using Pt\Ti\Pt\Au as the bonding pads metal stack, isolation is higher than 70 volts between typical bonding pads. However when the temperature was raised to above 200 °C, and a 56 volts reverse bias was applied to the diode, the leakage current between the pads went way above 10µA and thus did not enable to measure a breakdown voltage higher than 30-40 volts.

The poor isolation of the bonding pads at high temperatures gave the motivation for future development of a process that uses Silicon Nitride as the base for the bonding pads rather than the GaAs.

Up to now, a feasibility study of pads on Silicon Nitride has been done in the form of a short loop experiment on mechanical grade test wafers. In the framework of this experiment, Argon surface treatment was applied to achieve acceptable pads adhesion to the Silicon Nitride. Metal stack was also changed to Ti\Pt\Au compared to Pt\Ti\Pt\Au in the baseline process. Electrical measurement of the breakdown voltage between the pads at room temperature showed that the breakdown voltage between pads on Silicon Nitride is as high as 32 volts for a distance of 10µm, compared to 11 volts between pads on GaAs. Bond pull test showed mean breakout force of 11g. That is higher than the mean breakout force achieved with pads on GaAs. Accelerated life test at elevated temperatures and a reverse bias stress of 56 volts showed leakage current between pads of less than 10 µA at temperatures up to 225 °C.

ELECTRICAL PERFORMANCE

Electrical testing included the measurements of process control monitors of the anode and cathode contact resistance, epitaxial layers sheet resistance and passive elements properties mainly TFR sheet resistance and MIM capacitance. Some isolation patterns were implemented to measure the isolation properties of different structures of the bonding pads. The diodes were reverse bias DC characterized

to measure the breakdown voltage at 10μA. S parameters measurement was taken from 0 to 50 GHz for a reverse biased diode at –5 volts and forward bias of 20 mA (Fig. 4,5).

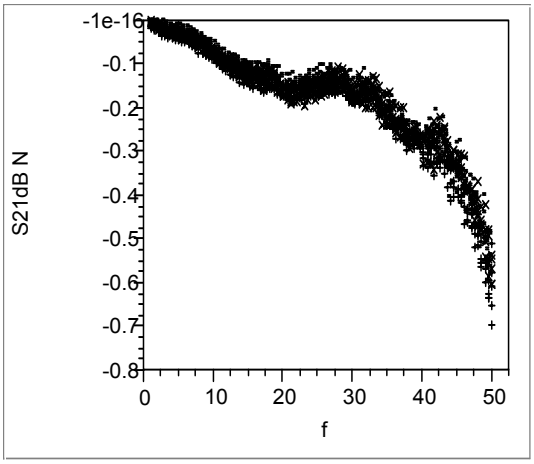

Figure 4 – 50 μm diode – Insertion Loss at –5 volts Reverse bias

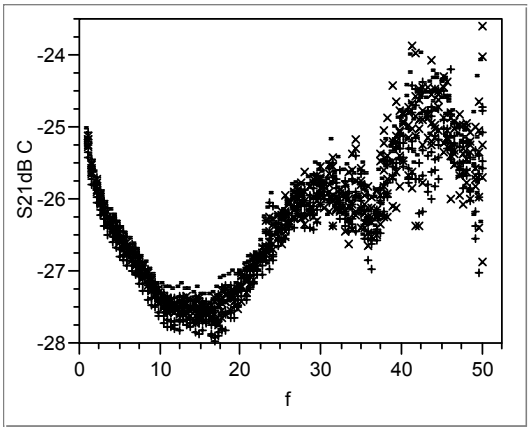

Figure 5 - 50 μm diode – Isolation at 20mA forward bias.

The series resistance of the diode is calculated from S-parameters of a micro-strip shunt diode. The transmission line contribution to the S-parameters is de-embedded by normalizing the S21 measurement of the diode in forward bias of 20mA to the S21 measurement of the diode in reverse bias of –5v.

When the diode is closed:

$$V_{out} = 1/2\, V_{in}$$

Then the diode's series resistance is:

$$Rs = \frac{Z_0}{2\left(\frac{1}{S21_{nor}} - 1\right)}$$

Where:

Rs - Diode Series resistance,

$$S21_{nor} = S21_{FwdBias} / S21_{RevBias}$$

$Z_0 = 50\ \Omega$,

RELIABILITY

Life test according to 10% R_{on} change failure criteria exhibited the MTTF of 140h at 200º C and anode current density of 17 kA/cm^2. This result is considerably greater than the MTTF of ~80h for typical devices of this kind [3].

CONCLUSIONS

A process for the fabrication of PIN diode has been presented that incorporates thin film resistors into the process flow.

The process is also capable of implementing fine structures for passive elements such as Lange couplers.

PIN diode performance is comparable with state of the art PIN diodes of the same features and enables the fabrication of high power switches with low losses and high isolation.

Diodes MTTF is 140h that is longer than typical devices of this kind.

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[3] Kenneth Decker, Private communication.

ACRONYMS

CPW: Co- Planar Wave-Guide
TFR: Thin Film Resistors
MIM: Metal-Insulator-Metal
CD: Critical Dimensions
PEB: Post Exposure Bake

