Cycle Time Reduction During Electroplating of Through Wafer Vias For Backside Metallization of III-V Semiconductor Circuits

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Keywords: through wafer vias, cycle time reduction, electroplating, gold-sulfite

Abstract:

The cycle time for electroplating through wafer vias (TWVs) has been reduced by 50% with little to no loss in plating thickness and uniformity by adjusting the plating parameters through design of experiments (DOE) studies. By optimizing the mechanical parameters of the plating tool, the power supply parameters, and the bath component concentrations, the studies showed that the current density could be doubled.

Introduction:

A TWV is a via connection from devices on the front side of the wafer to a completely metallized backside. The TWVs reduce electrical resistance and inductance to ground and reduce thermal resistance, allowing smaller die sizes and providing high power capability. Analog devices such as power amplifiers and monolithic microwave integrated circuits (MMIC) require the use of TWVs for minimization of impedances to obtain high power efficiency. (1)

The TWV metallization typically begins with the sputter deposition of a gold seed layer, followed by the electroplating of a thicker gold layer. (2) The primary costs of the electroplating process come from capital expenditures and from the cost of gold. Reducing the amount of gold deposited has often been viewed as the primary cost savings technique, and has been accomplished by reducing the current density used during deposition. However, with lower current density comes increased cycle time. To avoid additional capital expenditure during a production ramp, it became necessary to significantly decrease the plating time in order to increase wafer through put. Hence, the goal of this work was to reduce the gold plating cycle time, while maintaining low via resistances and high across-wafer uniformity.

Experimental:

The wafers used for this study were 100 mm GaAs wafers, thinned to 100µm, with 60µm diameter vias having nearly vertical sidewalls. Wafers were plated in a Semitool Equinox fountain system, with the Enthone gold-sulfite-based Neutronex 309 bath in a pulse-plating mode.

Baths were freshly prepared for the study of the bath chemistry and were used without any pre-treatment or conditioning. Separate baths were prepared for each test unless components could be added to a prepared bath to achieve the next required concentration.

Several factors were kept constant throughout all three DOEs. The anode to cathode ratio and the anode to cathode distance were not varied. The bath temperature was used at the vendor's recommended value of 50°C. Although important, the specific gravity (or Baume) of the bath and the bath age were not included in these studies.

Due to the variations in the composition of each bath, the Baume at each DOE condition varied considerably. The studies of the power supply and mechanical parameters were conducted on relatively new baths that were being used in production.

Jmp™ software was used for the statistical analysis of the data. The significant factors were identified using a step-wise regression, considering all first and second order interactions. A least squares model was then created using factors with Prob > | t | less than 0.1.

Twelve process control modules (PCMs) distributed across the wafer were used to test via resistance using a dc parametric tester. The via resistance (R_v) and standard deviation (R_v-SD) of the PCMs measured the amount and uniformity of gold plated in the vias. In addition, the step coverage (SC) was measured by cross-section and scanning electron microscope (SEM) images. Step coverage is the ratio of the thinnest point of the plate in the via to the thickness of the field on top in percent.

Results and Discussion:

An initial screening DOE showed that the plating time could potentially be cut in half by doubling the current density without a large sacrifice in plating thickness. The process was then optimized with full-factorial or partial-factorial studies of the power supply, mechanical parameters of the plating tool and the bath component concentrations.

DOE 1: Power Supply

The pulse plating parameters controlled by the power supply include the peak current density (CD_p), the ratio of time current is on to the total cycle time, or duty cycle (DC), and frequency (reciprocal of the total time of one cycle). (3) The CD_p and DC combine to determine the average current density (CD_{av}) which determines the overall plating time.

The average current density was the most significant power supply parameter, and affected both R_v and R_v-SD.

$$CD_{av} = CD_p * DC$$

= Peak current density * Time current on / Total cycle time

For CD_p = 0.8 amps with DC= 25%, CD_{av} = 0.8 * .25 = .200amps. There was little correlation with peak current density and duty cycle individually; a higher peak CD with longer DC or a lower peak CD with a shorter DC giving equal CD_{av} produced the same results.

The CD_{av} range giving the lowest R_v is ~ 3-4 mA/cm^2, above which R_v climbs quickly, as shown in Figure 1A. The choice of working CD_{av} is dependent upon the acceptable values of R_v defined for the device being plated. We found that for CD_{av} up to 6 mA/cm^2, R_v stayed below the limits set for our devices. But as the CD_{av} increased, so did the R_v -SD, thereby limiting the choice for operating CD_{av}.

Frequency showed a small effect, lowering R_v-SD slightly as the current density increased as shown in Figure 1B.

The CD_{av} adopted was 3.2 mA/cm^2, which resulted in an across-wafer uniformity of 1.5-1.7 mOhms.

A.

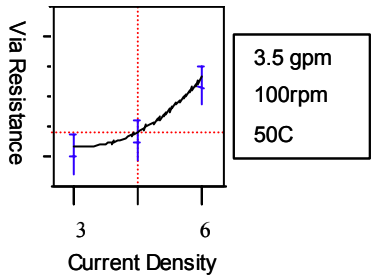

Figure 1. A) Effect of average current density on via resistance.

B.

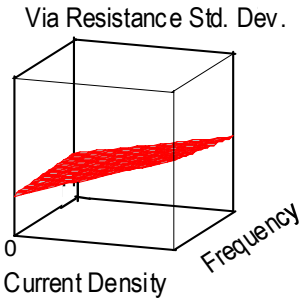

Figure 1. B) Effect of average current density and frequency on R_v -SD.

DOE 2: Mechanical Parameters

For the second DOE, the wafer rotation rate, solution flow rate and wafer oscillation were varied. The current density was also varied in order to determine the effect of each mechanical parameter coupled to current density.

The results showed that current density, wafer rotation and wafer oscillation were all significant factors for via resistance. Increasing the speed of wafer rotation was the most significant factor, and improved both via resistance (R_v) and the across wafer uniformity (R_v-SD). In addition, introducing a wafer oscillation slightly improved R_v, and increasing the bath flow rate slightly improved R_v-SD, as shown in Figure 2.

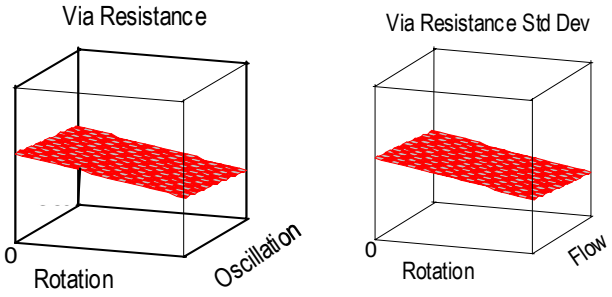

Figure 2. Left) Effect of rotation and oscillation on R_v. Right) Effect of rotation and flow on R_v -SD.

DOE 3: Bath Chemistry

In the final DOE, the concentrations of the bath components, gold, conducting salts, K_4P, brightener and pH, were varied to determine chemical effects on the via resistance and across-wafer uniformity.

The physical parameters held constant for this study were 3.5 gallons/minute flow rate, 50C, 100rpm rotation rate, and 3.2 mA/cm^2 current density with no oscillation.

R_v was reduced by increasing the gold and decreasing the brightener concentrations, while the R_v-SD was reduced by decreasing the gold and increasing the brightener concentrations, as shown in Figure 3. Unfortunately, in this case, the two components worked against each other. However, since the magnitude of the effect of the brightener is small and the acceptable operating concentration range is wide, it was easy to choose a working, or target concentration.

Selected samples were cross-sectioned and, the plating thickness was measured. Step coverage, SC, the ratio of the thinnest to the thickest plating, was calculated for vias at the center and on the edge of the wafer. Then the edge-to-center ratio was calculated to give a measure of the across-wafer uniformity. The values of SC ranged from 13 to 46%, while edge-to-center ratios ranged from 1.2 – 3.5, the ideal being 1.0. The best uniformity from the selected samples was at high gold and high conducting salts concentrations, with no brightener. Based on all the data, a compromise was reached between R_v and R_v-SD, using a relatively high gold concentration, a high conducting salt concentration, the vendor recommended K_4P concentration and a low brightener concentration.

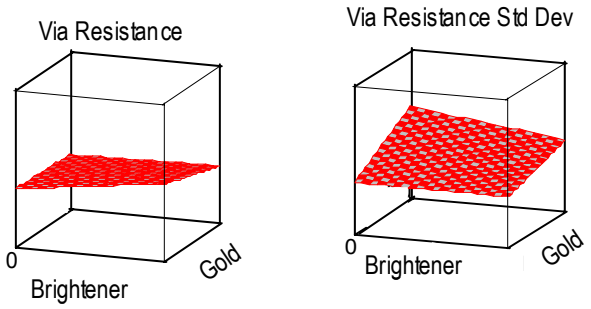

Figure 3. Effect of gold and brightener concentrations on left) R_v and right) R_v -SD.

Conclusion:

The new process implemented into production used the most optimum conditions possible from each DOE, while taking the through put requirements into account. Examples of typical plated TWVs are shown in Figure 4; one using the original process, the second using the optimized faster-plating process.

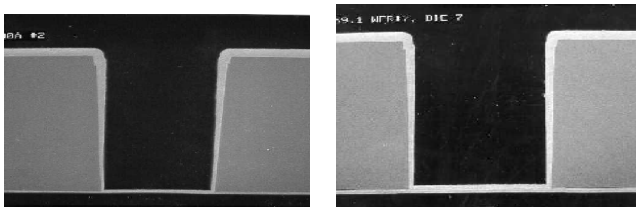

Figure 4: Plated TWVs from original procedure (left) and the optimized, faster plating recipe (right). Both photos are of 60μm vias.

Figure 5 compares the results of the optimized higher current density recipe with the original recipe in plating actual production lots. As shown, the optimized process exhibits excellent statistical process control for both via resistance and uniformity, while reducing the plating time by half.

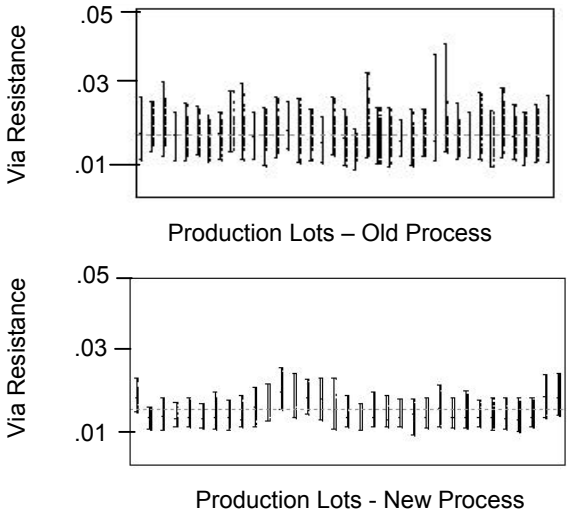

Figure 5. Comparison of SPC charts from the original and the optimized process.

References

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