Characterization and Control of Galvanic Corrosion During GaAs Wafer Photoresist Processing

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ABSTRACT

The occurrence of galvanic corrosion on compound semiconductor substrates with exposed metal has been observed as deleterious device effects.[1-7] Noble metals, e.g. gold, platinum, etc., in contact with exposed GaAs can induce undesired galvanic etching during wet process steps and result in surface irregularities that adversely affect yield. This phenomenon can occur when stripping photoresist using an aggressive wet chemistry. Rinsing steps that use de-ionized (DI) water can make matters worse.[1-3,5-7] Control and minimization of compound semiconductor and metal corrosion has received much attention in wafer fabrication. Some facilities have used electrical measurements or SEM (scanning electron microscopy) observations to characterize and alleviate corrosion issues. For photoresist mask strip steps, some facilities avoid problems by choosing a corrosion-safe chemistry, which may not necessarily provide optimum performance. Unfortunately, challenges in removing tenacious organic residues exist, especially from deep ultraviolet (DUV) and hard-baked exposures. Although residue removal typically involves more aggressive chemistries, substrate protection and cleaning efficacy can be achieved. Using novel chemistry formulations and process techniques, galvanic corrosion can be controlled. This paper characterizes GaAs based corrosion near ohmic and gate metal layer features and shows how it varies with the choice of chemistry and the addition of water due to absorption or rinsing.

INTRODUCTION

Photoresist stripping, metal lift-off, and related polymer removal processes in compound semiconductors may use commodity solvents, such as n-methyl pyrrolidone (NMP) or acetone.[6,8] Residue and metal stringers, which bridge the edge of the resist profile to the device, may necessitate a second cycle of solvent or high pressure DI water spray to ensure complete removal.[6] However, spraying can promote the movement of contamination from one spot to another and damage sensitive structures. Also, prolonged exposure to chemistry and DI water can result in galvanic corrosion to the semiconductor surface or ohmic metal contacts.[1-7,9] The SEM photos shown in Figure 1 indicate the progression of corrosion on AlGaAs immediately next to the delta gate metal lines (Ti/Pt/Au) as it is moves through the resist stripper chemistry and DI water rinse.

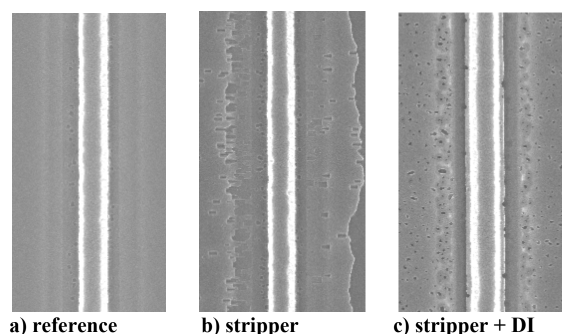

Figure 1: SEM photos of Ti/Pt/Au gate metal on AlGaAs showing the progression of galvanic corrosion observed as pitting and "mouse bites".

In addition to the use of SEM[1,5,6,10-14] to characterize corrosion pathways, several other techniques do exist, including TEM,[3,9] DC on-wafer electrical measurements,[1-5,9] and surface depth profiling with a stylus based system[3] or atomic force microscope (AFM). Depending on the process circumstances, observation of galvanic corrosion can vary from large pits (i.e. voids) to a subtle roughening of the surface. The nature of the condition will depend upon the ingredients in the chemistry, e.g. base, acid, or reactant, and how that material may swing the pH and conductivity of the DI water used as a post-strip rinse.

For positive resist stripping, solvents containing alkanolamines, such as monoethanolamine (MEA) and diglycolamine (DGA), are popular choices.[14-17] Other stripping constituents include NMP, dimethylsulfoxide (DMSO), dimethylacetamide (DMAC), sulfolane, and dimethylforamide (DMF).[15-17] Although some stripping formulations may perform well, be stable, and water rinse-able, they may also require heating to 90-120°C in order to effectively remove hard-baked resist films.[15-17] When working with substrates containing exposed metals, any alkanolamine formulation should include inhibitors since alkanolamines aggressively complex (attack) transition metals, such as copper and aluminum.[14-19] This behavior may explain the slow corrosion (etching) of exposed GaAs observed when using NMP/ MEA based resist stripping mixtures.

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Chemical exposures at elevated temperature can become lengthened during certain metal lift-off processes. Depending upon how the mask is designed, access to the underlying resist may be limited. Although not always practical, the ideal lift-off process will offer large access areas for chemical penetration. Figure 2 shows a metallized GaAs wafer (left side) and the access areas (right side) for a solvent to facilitate a lift-off process.

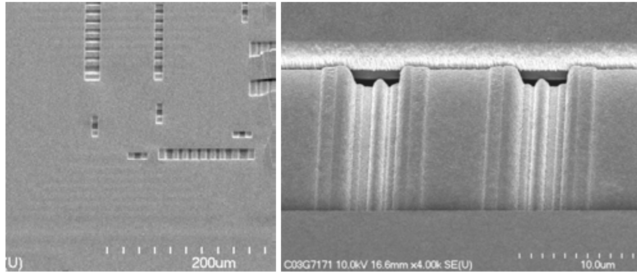


Figure 2: SEM photos of Ti/Pt/Au blanket gate metal on a positive photoresist masked GaAs wafer (left) and small access areas (right) for chemical penetration to facilitate metal lift-off.

In some instances new tooling can be implemented in order to improve process steps. High frequency ultrasonic agitation has been shown to be compatible with delicate front-side structures, such as air-bridges, enabling it to be used for wafer/ carrier de-bonding, cleaning, and metal lift-off.[14,20] Ultrasonic agitation facilitates rapid processing at reduced temperatures and minimizes exposure time which may mitigate galvanic corrosion effects. The effectiveness of utilizing 170 kHz ultrasonic agitation for as little time as 1 min to clean complex structures is shown in Figure 3.

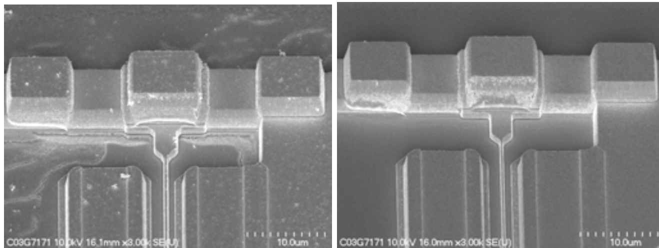


Figure 3: SEM photos of Ti/Pt/Au metallized areas on a GaAs wafer with photoresist residue and tape lift-off particles (left) and following a 1 min ultrasonic agitation in a solvent stripper at 170 KHz with the generator set at low power (right).

In order to be truly compound semiconductor wafer process compatible, high performance photoresist wet stripping chemistries need to be designed corrosion-safe with high selectivity while being aggressive enough to remove tenacious organic residues. The formulations must also be tailored for subsequent rinsing, such that semiconductor or metal corrosion does not occur.[14-19] This paper attempts to characterize GaAs based corrosion near AuGe/Ni/Au ohmic and Ti/Pt/Au gate metal features and show how undesired galvanic etching effects vary with the choice of chemistry and addition of water.

EXPERIMENTAL:

Several GaAs wafers (100 mm) went through a standard M/A-COM implant MESFET process, which includes a multiple dose silicon (Si) n-type implant and a boron (B) isolation implant. After the Si implant and rapid thermal anneal (RTA) steps, an AuGe/Ni/Au ohmic metal stack, with the AuGe at the eutectic concentration was thermally evaporated onto a positive resist masked wafer surface. The photoresist was stripped and the wafer rinsed using an acetone/ isopropanol (IPA) process. The ohmic metal stack was annealed at 370°C using a hotplate alloy track. The B isolation implant was done utilizing a positive resist mask. Before being selected for experiment use, the wafers from three different lots utilizing different mask sets were rejected from being used as product wafers at the post B implant process control monitor (PCM) electrical test step.

A 0.5 µm i-line stepper photolithography process was used for defining the delta style gate fingers. Prior to the Ti/Pt/Au electron beam (E-beam) evaporation, the gate regions of the wafers were single recessed using a tartaric acid based wet etch solution. Some wafers did not undergo gate recess prior to E-beam evaporation. After E-beam gate metals evaporation, the wafers were sent from M/A-COM to General Chemical Corporation (GCC) for the photoresist strip/ gate metal lift-off solvent chemistry experiments. GCC used a variety of chemistries, including GenSolve™, a proven line of chemistries for GaAs processing,

Transmission Line Model (TLM) contact measurements[21] were made before the gate definition process steps and after the solvent chemistry experiments on ten (PCM) sites across each wafer. The spacings between the linear array TLM ohmic contact pads, which were 40 µm long, were 5, 10, 15, 30, and 40 µm, and the structure was 100 µm wide. A SiN_x layer was not deposited to passivate the gate region, and TLM electrical measurements were made after the resist strip/ gate metal lift-off experiments.

The chosen resist strippers comprise a range of pure solvents and blends that closely match products used in the market place for semiconductor wafer processing. The solvents include linear and cyclic ketones (acetone, NMP, BLO, etc.), amides (DMAC, DMF, etc.), and sulfoxides (DMSO, $DMSO_2$, etc.). Additives that are commonly used include amines that vary between low molecular weight (LMW) alkanolamines, such as MEA, quaternary amine hydroxides, such as tetramethylammonium hydroxide (TMAH), and high molecular weight (HMW) amines, which can include cyclic and bicyclic varieties. Halogens found in strippers include fluorine, iodine, and others used to facilitate the removal of back-sputtered noble metal on organic. Unless otherwise indicated, all chemical blends used for this experiment are anhydrous (no water) since water addition may encourage galvanic corrosion. Table 1 describes the products used for this study.

Table 1: Chemistries used for the metal lift-off survey and subsequent testing. Each wafer # here is referenced in Table 2, which summarizes the SEM, ICP, and electrical test results. RT stands for room temperature.

Wafer #	Chemistry
1	Linear/cyclic ketone (RT)
2	Amide
3	Cyclic ketone + H_2O (5% w/w)
4	Amide + halogen
5	Cyclic ketone + LMW amine
6	Cyclic ketone + quat amine hydroxide
7	Sulfoxide + quat amine hydroxide
8	Amide + HMW amine
9	Amide + HMW amine + halogen

Prepared GaAs wafers with metal were immersed into vessels containing the noted chemistries in Table 1. They were chosen based upon GCC's experience in GaAs sensitivity, GenSolve™ as safe solvents, and knowledge of competing products. The conditions were 80-90°C for 30 min followed by an ultrasonic agitation at 170 KHz at a low generator setting for 1 min. Each wafer was then rinsed in IPA, dried, TLM electrical tested, and submitted for SEM analysis. The stripper solutions were retained for inductively coupled plasma (ICP) metals analysis.

Additional testing was conducted to evaluate the effects of water absorption and rinsing and to further demonstrate ICP metals analysis as a rapid screen for galvanic corrosion. Selected chemistries were tested with additions of water ranging from neat form (0% H_2O) to near 20% (w/w). A different mask set of wafers were used at similar conditions as outlined previously. The solutions were retained for ICP metals testing.

RESULTS:

SEM analysis of the wafers focused on areas of potential galvanic occurrence between dissimilar metals. Noble metal surface areas that are large in comparison to the exposed GaAs substrate are sources of galvanic corrosion. This is most likely to occur in the FET (field effect transistor) regions as shown in Figure 4 (left). The FET contains a series of noble metal gate fingers (Ti/Pt/Au) and ohmic contacts (AuGe/Ni/Au) adjacent to small exposed GaAs substrate areas (Figure 4, right photo).

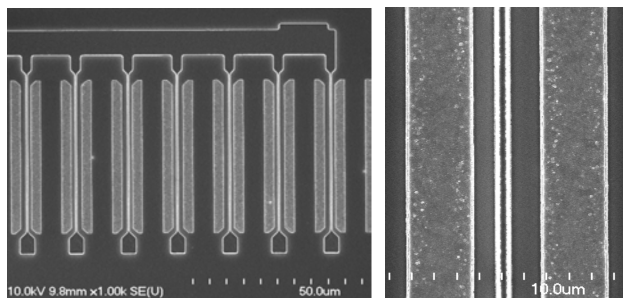
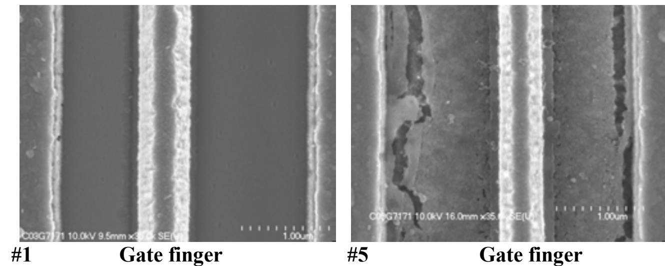


Figure 4: SEM photos of a FET region showing gate finger locations (left) and a closeup of a gate finger sandwiched between ohmic metal pads (right).

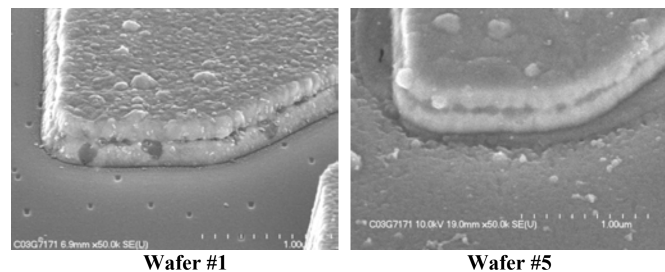
Higher magnification SEM photos of these gate finger regions revealed varied observations. Although some irregularities were evident on the metal, a focus on the GaAs substrate region at the base of the metal found evidence of corrosion. In Figure 5, a SEM photo of the gate finger region in wafer #1 indicates an acceptable appearance (left), whereas wafer #5 is severely attacked (right).



#1 Gate finger **#5 Gate finger**

Figure 5: SEM photos of GaAs wafer #s 1 and 5. For each photo Ti/Pt/Au gate fingers are in the middle and the AuGe/Ni/Au ohmic contacts are on either side. Normal gate recess wet etch is noted in wafer #1, while corrosion appears to be significant along each edge of the finger in wafer #5.

Tilting the sample in the SEM revealed additional information about the etch/ corrosion areas along the ohmic contact metal/ GaAs surface boundary. In Figure 6, the drain ohmic metal contacts are revealed showing an acceptable appearance for wafer #1 and serious recession in wafer #5.



Wafer #1 **Wafer #5**

Figure 6: SEM with tilt of wafer #s 1 & 5 that provide a closer look at the ohmic contact/ GaAs substrate boundary. For wafer #5 significant etch/ corrosion is clearly visible adjacent to the ohmic metal pad.

All of the wafers listed in Table 1 were evaluated by SEM and observed for the presence of corrosion. The review included top views of the gate fingers (Figure 5) and tilt angle views of the ohmic metal to GaAs boundaries (Figure 6). The attribute results are listed in Table 2 as SEM corrosion.

The TLM measurement results from ten PCM sites taken for each GaAs wafer before and after chemical exposure were averaged and compared. A percentage calculation (%R) was performed to give a value respective of the before result. Therefore, high values of %R reflected a small change in the average TLM before vs. after results, while values equal or near zero signified a large change indicative of detrimental corrosion.

Table 2 compares corrosion as observed by SEM photos, values of %R, and ICP metals analysis for the corresponding stripper solutions. A correlation is apparent between these

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three results. Namely, the appearance of corrosion in the gate regions indicates a performance drop as a reduction in %R and material loss to be detected by ICP as dissolved metal.

Table 2: The SEM attribute results and the corresponding TLM electrical data are given below. Electrical is expressed in terms of a % of the original (before) TLM average result. The ICP metals analysis on the corresponding stripper solutions is expressed in ppm (parts per million) for total metal elements (i.e. Ga, As, etc.).

Wafer #	SEM Corrosion	%R	Metal (ppm)
1	No	98.56	0.00
2	No	96.01	0.00
3	Yes	83.13	4.28
4	Yes	0.00	11.61
5	Yes	24.32	0.07
6	Yes	0.00	22.67
7	Yes	0.00	11.72
8	No	99.47	0.00
9	Yes	0.00	30.95

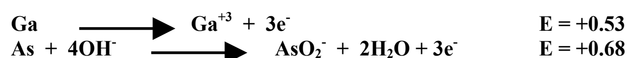
The effect of water addition to the stripper chemistry on GaAs corrosion is monitored by ICP metals analysis. The results in Table 3 show a trend of increasing metal dissolution with water addition. Limited effects exist for solvents, while the addition of certain amines will accelerate metal attack.

Table 3: Metals analysis by ICP on selected chemistries and the respective water additions in contact with metallized GaAs wafers. The mask set used varies from previous tables. All solutions are 80-90°C @ 30 min. Addition of H_2O is defined as: a) neat = 0% H_2O, b) 5% H_2O, c) 20% H_2O.

Chemistry	a) Metal (ppm)	b) Metal (ppm)	c) Metal (ppm)
Amide	0.00	0.02	1.91
Cyclic Ketone	0.00	0.01	0.65
Cyclic ketone + LMW amine	7.63	19.91	38.51
Amide + HMW amine	0.00	0.16	22.71

CONCLUSIONS:

Corrosion of GaAs wafers in the gate region was observed to occur when exposed to certain chemistries at temperature over time. Support for the theory behind galvanic occurence is explained by the electromotive series indicating *Ga* and *As* to exhibit positive oxidation potentials:



$$Ga \longrightarrow Ga^{+3} + 3e^- \qquad E = +0.53$$
$$As + 4OH^- \longrightarrow AsO_2^- + 2H_2O + 3e^- \qquad E = +0.68$$

The reductive part of the equation may be driven by the oxidizing agents in the chemistry, including hydroxide (OH^-) as produced by amines, halogens (F, I, etc.), and the ubiquitous presence of oxygen. Further, the addition of water increases solution conductivity, and enhance ionization. When these factors are combined with GaAs isolation in the gate region by comparative large areas of noble metal, the occurrence of galvanic corrosion is likely.

We have shown that characterization of GaAs corrosion for sensitive frontside wafer processing may include SEM analysis, electrical performance, and solution metal analysis by ICP. Although these techniques may be valuable, the authors suggest process plans to prevent corrosion. These include proper choice of a GaAs-safe resist stripper matched to the material to remove, a tool (i.e. sonics) for quality performance and reducing exposure time, and finally, the use of anhydrous rinse agents such as IPA or acetone.

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