Low Damage Dielectric Etching on GaAs Using a Helicon Wave High Density Source

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Abstract

An RF helicon wave high density plasma source has been used to develop a low damage SiO etch process for fabrication of submicron features on GaAs substrates. Etch rate and damage measurements were made on implanted GaAs substrates, coated with SiO deposited by RF plasma CVD. Increases in post-etch sheet resistance as low as 12% could be achieved using a CF4/O2 chemistry and 10% overetch. A 0.36μm gate structure was fabricated yielding a residue free, anisotropic etch, with an increase in critical dimension of 600± 100Å from the photolithography and excellent device characteristics. This represents the first demonstration of this etch technology in the fabrication of submicron GaAs devices for digital and mixed signal applications.

INTRODUCTION

The effort to reduce the minimum feature size and access higher operating device frequencies necessitates the use of high density plasma technology for high resolution, low damage, etch processes in III-V device fabrication. The demand for high density plasmas has been generated by the potential for achieving high etch rates and excellent anisotropy with low substrate damage.[1-3] These etch properties are achieved as a consequence of low operating pressures (<10 mTorr), high plasma density (>10^{11} cm^{-3}) and the ability to control ion energy and ion density with relative independence. Typically, ECR (electron cyclotron resonance) or ICP (inductively coupled plasma) sources have been employed. Etch processes based on ECR and ICP plasma generation have been systematically evaluated for GaAs and other III-V semiconductor material device development.[4-6] However, the use of helicon wave high density plasmas in the fabrication process for III-V semiconductor materials has been significantly less investigated. To our knowledge this is the first report of a low damage submicron gate oxide etch utilizing a RF helicon wave technology.

Silicon nitride or oxides are used ubiquitously in processing of III-V compound semiconductor devices for surface passivation. Conventional RF reactive ion etching (RIE) has been used for dielectric removal, but this technology suffers from a number of process limitations. These include the inability to decouple ion density and ion energy, higher operating pressures (limiting control over critical dimensions) and lower etch rates. Due to these issues ECR and ICP systems have been systematically explored as alternatives, with ICP becoming the most widespread technology used in III-V semiconductor processing. However, helicon wave high density plasma sources possess similar etch characteristics which should be optimum for III-V production applications.[7-9]

EXPERIMENTAL

The generation of an RF helicon wave high density plasma is based on the propagation of an RF electric field in a axially uniform magnetized plasma. The construction is based on 2 RF antenna loops driven 180 degrees out of phase and surrounded by a set of coplanar magnetic coils. The helicon resonance condition is obtained for high density plasma generation, when the induced wave field pattern propagates between the two antenna loops in one-half of an RF period.[9,10] Independently of the plasma generation, an RF bias may be applied to the downstream substrate stage allowing for relatively independent control of ion energy. In this study a Trikon production system was used equipped with an electrostatic chuck (ESC) operating at a temperature of 10C. The platten could be biased at 13.56MHz to extract ions at a controlled energy.

As a means to evaluate device damage in a single recess MESFET process for digital and mixed signal applications, GaAs substrates, implanted with a combination of SiF_3, Si and Be, were employed for measurement of changes in sheet resistance R_{sh}. A 1300Å layer of plasma deposited silicon oxide was applied for surface passivation and enhanced impurity activation during the subsequent implant anneal. Oxide thickness was determined by standard ellipsometry. Surface damage was evaluated by measuring the sheet carrier resistance using a Lehighton model 1310-R before and after etches. This investigation focused on the use of CF_4, O_2 and Ar as process gases, where Ar was used to aid in anisotropy and O_2 in reduction of residual surface polymers. The plasma was characterized using optical

emission spectroscopy, where a Luxtron model 1015 endpoint controller was employed, equipped with a scanning monochrometer and fibre optic cable mounted on a chamber window, where the line of sight would be < 1cm above the substrate stage.

RESULTS AND DISCUSSION

The etch rate and surface damage, at a pressure of 10mTorr, as a function of RF bias and source power, are shown in Figures 1and 2 respectively. In Figure 1, the platten RF bias power was varied while keeping the source power constant at 500W. Figure 2 shows results for variation of the RF source power with the bias power set at 5W. An overetch of 10% was applied in both cases based on endpoint time. As shown in Figure 1 the sheet resistance is well correlated linearly to the RF bias power. This is expected given an increase in the substrate self bias potential will directly increase ion energy and hence damage. Note the increase in R_{sh} could be limited to as low as 12% with 0W applied bias. This increase in R_{sh} is comparable to that obtained by wet etch removal of the SiO film. Similarly in Figure 2 R_{sh} is shown to be linearly dependent on source power, but diverging from this dependence at powers greater than 1500W. It was found that above approximately 1500W the etch rate saturates and at source powers as high as 2000W, residue was visually observed on the surface of the wafer. This may be due to sputter redeposition of polymer or other reactant etch species, given the inherent competition in etch process between sputter removal and redeposition of reactants.

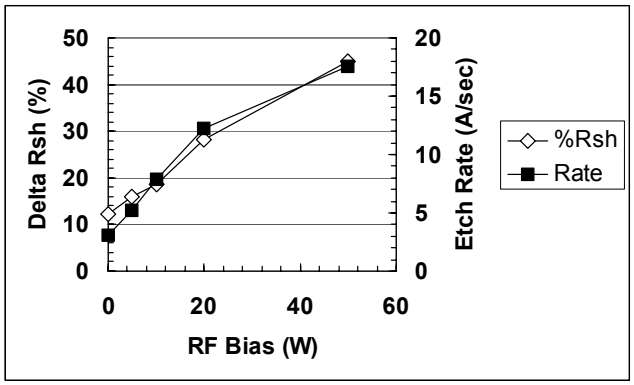

Figure 1. Etch rate and increase in Rsh as a function of RF bias power at 10mTorr. Source power was left constant at 500W.

To determine the influence of fluorine concentration on the oxide etch rate argon actinometry was employed.[11, 12] In this technique an inert tracer gas (Ar) is added to a compatible process gas (CF4) and the emission intensities

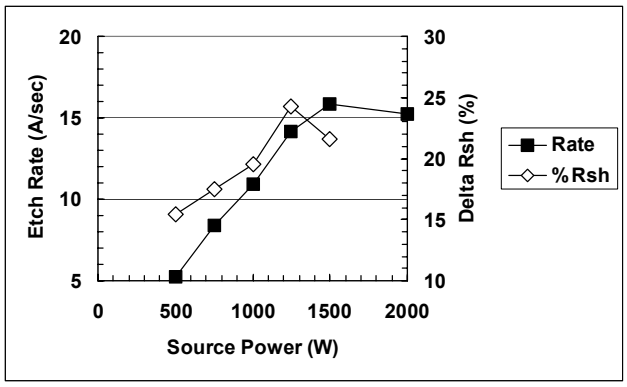

Figure 2. Etch rate and increase in Rsh as a function of source power at 10mTorr. RF bias power was left constant at 5W.

are measured as a means of determining the relative density of a specific plasma species. Figure 3 shows the relative intensity of the 706nm F emission line to the 753nm Ar line and etch rate as a function of source power. The etch rate is well correlated linearly to the relative concentration below 1500W source power. This result agrees well with data from other plasma etch systems, where SiO etch rate is dependent on the relative concentration of fluorine in the plasma.[13] At higher source powers the etch rate begins to decline for reasons discussed above, although the fluorine concentration continues to increase.

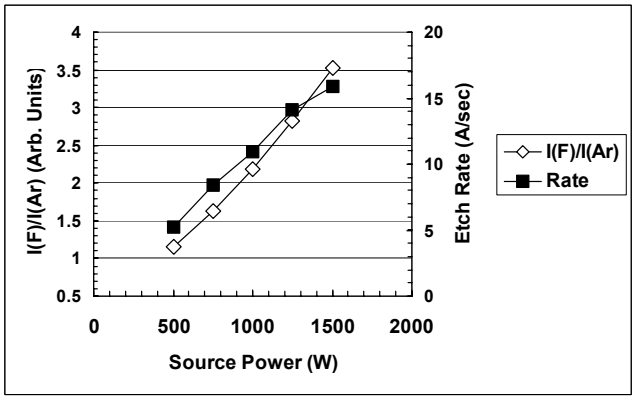

Figure 3. Etch rate and relative fluorine concentration at a pressure of 10mTorr and 5W RF bias power.

Figures 2 and 3 imply that ion saturation current as well as ion energy contributes significantly to semiconductor device damage for helicon wave plasmas. Figure 4 compares this data to measurements of ion saturation current by G.R.Tynan et al. at a pressure of 10mTorr and gives reasonable confirmation of this correlation as has also been noted for ECR etching systems.[14]

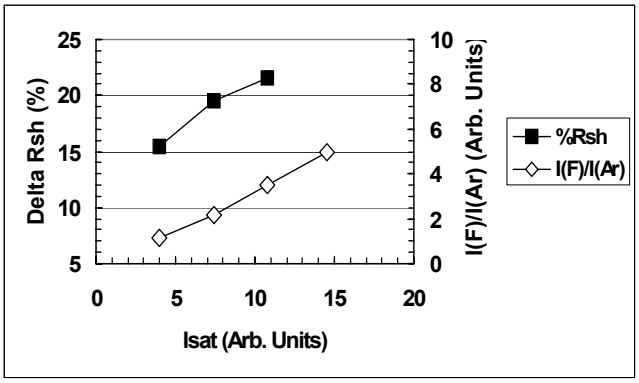

Figure 4. Effect of ion saturation current on induced semiconductor damage Rsh.

After initial characterization of the helicon wave plasma process optimization was completed using a statistical design of experiment. Parameters of CF4, O2 and Ar gas flow were varied with pressure and total flow rate. The RF bias and source power were minimized at 5W and 500W respectively based on the requirements of low damage with an acceptable etch rate (approximately 5Å /sec) for production throughput. A liftoff profile was created using a two-layer photolithography process in order to delineate the gate electrodes. A scanning electron microscope (SEM) cross-section of the optimized process is given in Figure 5. The etch bias was measured at approximately 600± 100Å with an overetch of 25%. The observed undercut was part of the photolithography process. The etch produced no surface residue using CF4/O2/Ar based processing with the helicon wave source and yielded excellent anisotropy in the SiO.

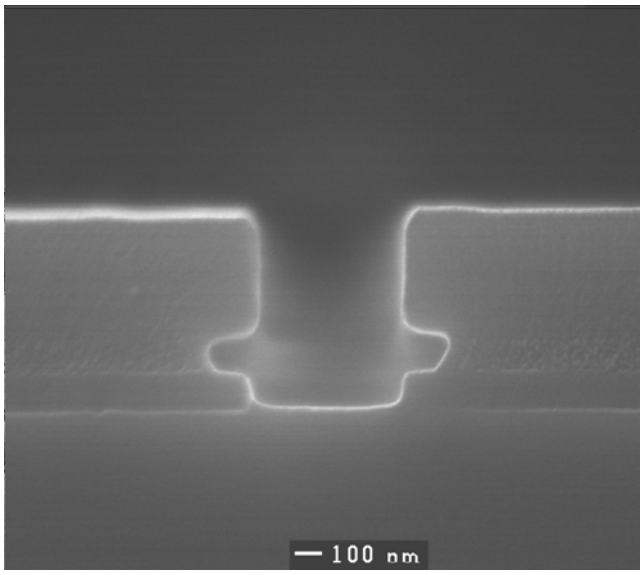

Figure 5. SEM cross-section of a representative gate profile after completion of the low damage etch. The undercut is part of the photolithography process.

CONCLUSIONS

Using this low damage etch process a 0.30µm image in photoresist was transferred into the 1300Å SiO film and subsequent device parameters evaluated. The critical dimension in the oxide film was 0.36µm ± 0.01µm. The 0.36µm MESFETs possessed a V_{th}=+0.30 ± 50mV, I_{max} =186 ± 20mA/mm and f_t=50.7 ± 2.7GHz for the E-mode devices and a V_p=-415 ± 74mV, I_{DSS}=67 ± 17mA/mm and f_t=42.5 ± 3.3GHz for the D-mode devices. These optically defined 0.36µm MESFETs with SiO surface passivation possessed similar performance characteristics compared to electron beam defined 0.30µm MESFETs with SiN surface passivation.

This study demonstrates the viability of RF helicon wave plasmas for low damage gate dielectric etching in the fabrication of III-V devices. This is a new application for this technology, which allows for the development of low cost, high throughput production processes for devices requiring submicron critical dimensions.

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