Integrated Microsystems: The Next Technology Transition

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Abstract

Over the past 30 years there has been an incredible explosion of solid state technology that has allowed for storage and processing of, and interaction with, massive amounts of information. To extend this capability for the Department of Defense, DARPA has launched a major initiative to start the next technology revolution, to establish Integrated Microsystems. These new microsystems will integrate sensing, processing, actuation and power management functions to achieve multispectral functionality, adaptability in response to a changing environment, and real time data analysis. This revolution will result in commercial and military products that exploit component integration and performance in novel ways.

INTRODUCTION

Gallium arsenide (GaAs) has been the "technology of the future" with respect to digital electronics for the past thirty years, since it has never been able to supplant silicon (Si) as the dominant semiconductor in digital integrated circuits [1-3]. The higher electron mobility of GaAs has not resulted in a consistently overwhelming advantage in circuit capability for GaAs devices over Si devices, partly due to the rapid pace of improvements in silicon technology. This highlights the point that device level performance alone is not the key metric, but rather circuit level capability, as measured by speed, power, and precision, are the factors that drive market acceptance. For example, when researchers from IBM first created Si devices using a 1 μm process, their performance rivaled state-of-the-art GaAs semiconductors at the time [4]. While GaAs manufacturing has made great strides since then, Si has managed to keep pace. In 2002, IBM researchers announced a silicon device with f_T of 148 GHz, using silicon-on-insulator (SOI) and a 0.13 μm process [5] while III-V technologies reported InP PHEMTs with f_t exceeding 500 GHz [6].

Junction-level results may generate great excitement, but technology adoption is ultimately driven by yielded manufacturing cost, integration capability, performance and market size. The emergence of RF SiGe and CMOS/SOI, both with wafer costs of less than \$4/cm^2 [7] and with the ability to integrate greater than 100 million transistors [8], leads us to ask once again: Is there a role for III-V component technology in areas other than analog and millimeter wave electronics?

Aside from niche applications, III-V technology has a critical role in future systems but not as an extrapolation of where the technology exists today. Rather a revolution, that we term the Integrated Microsystem, is emerging that will include III-V and silicon based components on a common three-dimensional hardware platform.

THE CHALLENGES FOR CMOS

Extending current levels of CMOS scaling and integration, within five to ten years conventional electronics will enable systems containing perhaps a trillion transistors in roughly a liter of volume and dissipating less than 100 watts or so [9-11]. This is about the same complexity as the human brain, and is the kind of complexity that Integrated Microsystems will exploit [12].

Smaller feature sizes have led to tremendous gains in CMOS performance [13,14]. While CMOS junction scaling will likely continue, future system concepts will be limited by component thermal dissipation, interconnect capacitance, clock synchronization and design verification [15]. Removing heat becomes more of an issue as feature sizes decrease because of the simultaneous higher electric field densities and reduced volume available for heat transfer [16]. At very small scales, increases in interconnect delay negate decreases in gate delay, since smaller wire cross sections and smaller wire pitch increase the resistance and capacitance, and thus RC delay, of the interconnects [17]. Clock synchronization becomes a major limiter in the areal growth of high-frequency ICs when the maximum-allowed

clock signal line exceeds the size of the chip [18]. Finally, the complexity of circuits possible at smaller CMOS scales makes design verification and testing problematic. As a result of the non-negligible interconnect delays and uncertainty in clock synchronization, current modular design tools may be inadequate in a small-scale, highly integrated regime [19]. It is clear that new circuit design techniques are needed to continue the current CMOS system scaling trend [20].

THREE DIMENSIONAL CIRCUITS

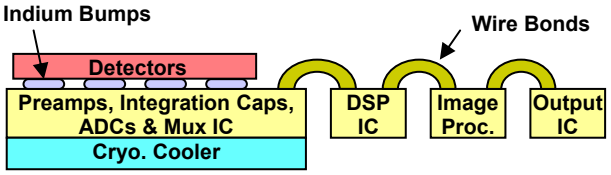
Three-dimensional circuits (3-D) play a key role in the development of Integrated Microsystems. The emergence of 3-D device-level heterogeneous integration will enable volumetric system scaling and open a new revolution in microelectronics [17,18,20-22]. 3-D integration was demonstrated as early as 1979 [23], and some limited research on 3-D device fabrication and characterization was reported throughout the 1980's [24-29]. But, now that standard CMOS scaling is nearing limits there has been renewed research activity [30-33], and commercial interest [34,35].

In a 3-D system, an entire circuit is divided into a number of blocks, and each block is implemented on a separate semiconductor layer. The layers are stacked on top of one another and connected via vertical interlayer interconnects. This allows for a much smaller chip footprint, and can alleviate the clock synchronization issue by replacing long horizontal traces with much shorter interlayer connections. In addition, with horizontal area at less of a premium, interconnect pitch can be increased, which reduces the capacitance and improves overall chip performance.

The stacked layers in a 3-D chip need not have the same performance characteristics, or even architecture. In principle, they can have different voltages, they can use synchronous or asynchronous logic, and they can even use different materials. Thus, rather than simply making a single 2-D chip smaller or faster by breaking it into blocks, 3-D integration can also be used to fabricate entire systems of chips in a single package. This is the concept of the Integrated Microsystem.

Perhaps the first example of an Integrated Microsystem with heterogeneous integration will be applied to a multispectral imaging array. In a typical CCD sensor system, imaging pixels are connected laterally with A/D converters, digital signal processors, image processors, and output ICs by chip-to-chip interconnects. This results in a large device with a relatively small active area. The sampling rate and resolution are limited by this interconnect approach. The Vertically-Integrated Sensor Arrays program (VISA) is designed to change that. Figure 1 shows a schematic diagram of traditional sensor electronics compared with the VISA design. VISA will create a layered IC, in which each layer represents one of the subsystems in a traditional sensor device. The layers are connected via strategically placed interlayer connections, effectively creating a three-dimensional chip. This will result in devices that are much smaller, with more effective area and higher readout rates than are available today, and will change the discussion about IC components from one about areal density to one about volumetric density. The feasibility of the interlayer connections has been demonstrated using 6-μm-wide tungsten plugs connecting layers spaced at 28 μm intervals, as shown in Figure 2 [36]. Progress is now under way to improve both operability and yield.

FIGURE I
A) TRADITIONAL SENSOR AND ASSOCIATED ELECTRONICS LAYOUT



B) VERTICALLY INTEGRATED SENSOR ARRAY
(PASSIVE FOCAL-PLANE ARRAY ELEMENT)

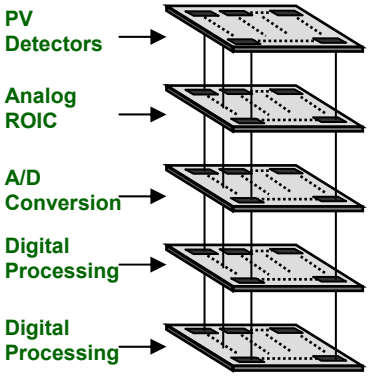
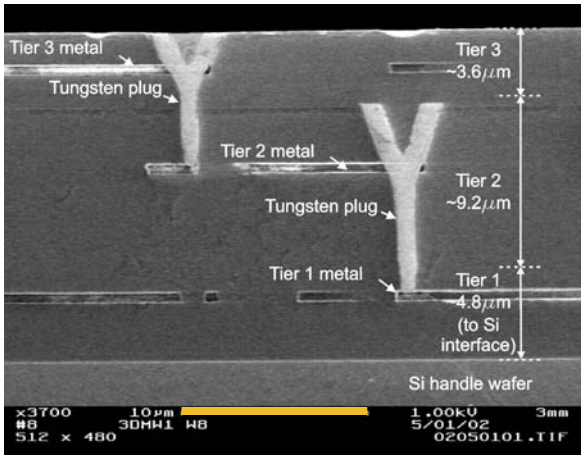


FIGURE II
ELECTRON MICROGRAPH OF CROSS SECTION OF A VISA CHIP, SHOWING SEMICONDUCTOR LAYERS CONNECTED BY TUNGSTEN PLUGS



CAPABILITIES ENABLED BY INTEGRATED MICROSYSTEMS

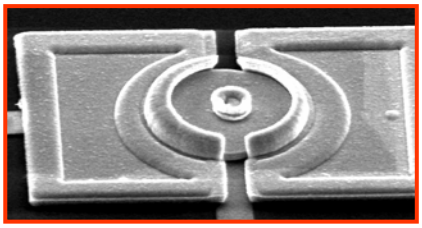
Today's battlefield is unpredictable, unregulated, dynamic, and increasingly asymmetric; tomorrow's battlefield will be even more so. The greatest opportunity in the next decade will be to use the sensing, signal processing and integration capability of Integrated Microsystems to build systems that sense and adapt to the environment across the full spectrum; that dynamically configure to the mission at hand; and that actuate elements of the environment with micro-scale precision. Such capabilities will enable spectacular autonomous and interactive systems that can reason, sense, communicate, and actuate in ways not previously possible. One example would be flexible receivers that can tune themselves automatically and capture signals opportunistically. Such a device would enable the development of systems that truly interact intelligently with their environments.

Leveraging CMOS performance, highly integrated mixed signal microsystems are being developed with low noise, low power consumption, advanced signal/data conversion, and high frequency digital synthesis [37]. Using integration approaches such as 3-D fabrication, signals from an imaging array can be brought directly to the readout circuitry without the need for subsequent processing. This will have an enormous impact in image quality and will enable, for the first time, building chip-level multispectral imagers.

Integrated Microsystems hold the promise of integrating photonic and optoelectronic components into traditional CMOS electronic circuits as well. 3-D integration of optical and CMOS circuits was demonstrated in 1995 [38], but today's emerging 90nm CMOS fabrication process appears to have the line smoothness to support wavelength-scale nanophotonic devices for the first time [39]. Fabricating high performance photonic circuits in a CMOS process will enable integration with CMOS electronics, yielding high performance VLSI nanophotonics and electronics on a single chip. This will be key to overcoming many of the latency, coupling, and bandwidth issues that limit conventional electronics, and it will find ubiquitous applications in everything from communications to sensors to RF photonics, and wherever photonics and electronics intersect.

One difficulty any highly-integrated system will have to overcome is in miniaturizing passive components, such as resonators, switches, capacitors, and inductors. The DARPA Nano-Mechanical Array Signal Processing program is taking on this challenge. Researchers are using MEMS techniques to produce arrays of nano-resonators that can be integrated with other components *in silico*. Figure 3 shows a working radial contour-mode disk resonator with 10 μm radius and Q=1,595 at atmospheric pressure [40]. Work is now aimed at coupling resonators like this together to make large arrays.

FIGURE III
1.14-GHZ SELF-ALIGNED DISK MICRO-MECHANICAL RESONATOR



CONCLUSION

DARPA has launched a major initiative to develop the supporting technologies to start the revolution of the Integrated Microsystems. This architecture will extend two-dimensional circuit scaling to volumetric integration and heterogeneously integrate sensing, processing, actuation and power management functions. The Integrated Microsystem will enable a new set of capabilities resulting in commercial and military products that exploit component integration and performance in novel ways.

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ACRONYMS

A/D: Analog-to-digital
CCD: Charge-coupled device
CMOS: Complimentary metal oxide semiconductor
DARPA: Defense Advanced Research Projects Agency
f_T: Transition frequency
GaAs: Gallium arsenide
IC: Integrated circuit
MEMS: Microelectromechanical systems
MTO: Microsystems Technology Office
RF: Radio frequency
Si: Silicon
SiGe: Silicon germanium
SOI: Silicon-on-insulator
VISA: Vertically Interconnected Sensor Array