High Bandwidth Devices: Faster Materials versus Nanoscaled Si and SiGe

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Abstract

We explore the use of InAs as an alternative to nanoscaled Si for future generations of high bandwidth MOSFET-based circuits. InAs has a high electron mobility. Its v_{sat} is theoretically 20 times higher than silicon's. Our modeling shows that an HBT could achieve f_T and f_{max} approaching 1 THz for an emitter-base and collector-base dimension of 0.5 μm x 4.0 μm (2 μm^2). A simple MOSFET model predicts an f_T of about 3 THz for a gate length of 0.1 μm. The model is consistent with known experimental measurements of InAs materials parameters. InAs technology may support ultra-fast devices at 90 nm and below, or performance at 90 nm comparable to strained Si and SiGe at 45 and 22 nm features. To support the integration of InAs devices with Si circuits, we are developing a high quality InAs epilayer technology using non-lattice-matched GaP substrates.

INTRODUCTION

Strained Si and SiGe MOSFET technology face fundamental limits towards the end of this decade when the technology roadmap calls for gate dimensions of 45 nm headed for 22 nm. This fact, and difficulties in developing a suitable high-K dielectric, have stimulated the search for alternatives to brute-force scaling of Si and SiGe MOSFETs. Prominent examples include nanowires, molecular electronics, and other "way out" prospects disconnected from manufacturable technologies. Researchers in III-V devices have made significant strides in ultra-high speed devices but face immense obstacles arising from density and the poor yield of complex circuits. Thus, Si MOSFET and bipolar technology is still king and may stay that way at least until I retire.

However, there may be a way to keep Moore's law viable: both fast-enough devices and manufacturability. The approach is to employ materials with more suitable ultra-high speed properties — extremely high mobility and saturated drift velocities — which can be integrated monolithically with current Si manufacturing technologies. This paper describes our work toward using InAs as the material of choice for this goal. We review the current performance versus dimension for Si, SiGe, MOSFETS and HBTs, and some III-V materials used as MESFET, HBT and HEMT devices. We show the modeling results for our ideal InAs HBT structure and MOSFET and MISFET structures and summarize the results to date on our InAs on GaP materials technology.

RESULTS AND DISCUSSION

MODELING RESULTS

We have modeled a target *npn* InAs HBT structure with a Schottky collector-up configuration. A description of the structure follows. The base doping and thickness are 1×10^{20} cm^{-3} and 50 nm respectively. The emitter region is a pseudomorphic layer of $Al_{0.75}In_{0.25}As$ graded from InAs in the "sub" emitter region doped to $>1\times10^{19}$ cm^{-3} to AlInAs at the base-emitter interface. The emitter depletion region is undoped and about 200 nm thick, to prevent the formation of a parasitic tunnel diode between the emitter and base. The conduction band offset between emitter and base is about 0.25 eV so that electrons launched from the emitter into the base will have a velocity of about 1×10^8 cm/s. This is needed so that the transit time through the base (5×10^{-14} s) is much less than the Auger lifetime of electrons in the base (1 ps), because even for an HBT, the gain is ultimately limited by the ratio of carrier lifetime to the base carrier transit time. The undoped, 200 nm $Al_{0.75}In_{0.25}As$ Schottky collector depletion region is graded from InAs at the base-collector interface to AlInAs to smooth out any band offset that could result in quantum mechanical reflection of electrons entering the collector. The metal Schottky contact to the collector depletion region has a barrier height of about 0.6 eV. We chose the collector-up configuration for processing and modeling testing considerations. We can use the metal Schottky contact as a mask to define the base-collector areas and emitter collector areas to be the same. The base-collector area is defined by selective etching back to the base layer, and the emitter-base area is defined by implantation through the base, with the implanted emitter being non-conductive while the base, with its high *p*-type Be doping, will remain highly conductive in the implanted region. (The details and schematic diagram of the structure are presented in the talk and full manuscript.)

Using the parameters above and the complete equations for f_t and f_{max}, including both inherent and parasitic resistances and capacitances, and assuming a v_{sat} of 2×10^8 cm/s in the

collector depletion region, and emitter-base and base-collector dimensions of 500 nm × 4000 nm, we obtain an f_T and f_{max} of 0.96 THz and 1.1 THz respectively, a beta of 120, and a V_{ECO} of 4 V. This result is displayed in Fig. 1 along with selected literature data for SiGe and SOI MOSFETs and HBT data for SiGe and selected III-V compounds and alloys.

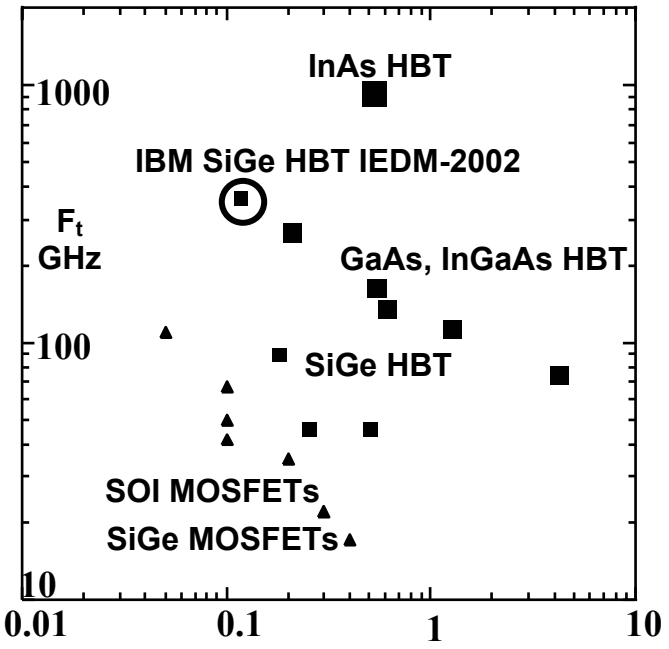

Fig.1. Cut-off frequency of various transistors v. emitter/gate widths in μm.

Two points should be made. First, Si and/or SiGe MOSFETs can only get to 100 GHz f_T at gate length dimensions well under 100 nm, and SiGe HBTs require 200 nm or less to get to 100 GHz compared to 500 nm for III-Vs.

Second, there is currently no practical solution for any Si or SiGe base transistor to get to f_T of 1THz, whereas InAs-based HBTs have a reasonable chance of getting there at 0.5 μm dimensions.

Finally, a simple model which does not include parasitic effects predicts an f_T of 3 THz for InAs MOSFETs at a gate length of 100 nm.

So, there are good reasons to explore InAs technology for ultra-fast electronics and possibility as a future alternative to scaled strained Si and SiGe transistor technology due to higher yield and lower costs expectations of not having to manufacture chips at the tens of nanometer dimensions.

TECHNOLOGY ENABLER

It should be noted that several industrial and national laboratories along with several universities have government agency funding to explore InAs-based transistor technology, yet none has achieved breakthrough performance. This is due mainly to the defects arising from use of non-lattice-matched substrates. InAs is not available as a low- defect substrate (the nearest match is GaSb, whose substrates are not stable in air) and has excessively high surface conductivity due to shallow donor surface defect states.

We have chosen to develop an epitaxial enabler for InAs devices using insulating GaP substrates. Even though there is an 11% mismatch between the lattice constants of InAs and GaP, GaP is nearly matched to Si. For this reason, we believe it will become practical to integrate InAs ICs either directly onto Si substrates or via an interface layer of GaP. Table I is a summary of the properties of our InAs grown on GaP.

TABLE I
PROPERTIES OF InAs ON GaP SUBSTRATES

- Mobility > 20,000 cm^2/V-s at RT after 2 μm of growth (Si is only 800 – 1000!).
- Uniform square array of 90° edge dislocations whose crossings are shallow donors (10^{13} cm^{-2})
- Threading dislocation density is 10^7 cm^{-2} after 2 μm of growth and a strain-layer superlattice
- Dislocation cores are shallow donors with a linear density of about 3×10^7 states/cm
- Atomically smooth surfaces, no "cross-hatch"

CONCLUSIONS

I have stated in the past, "Never seriously try to make it out of anything else if it has a chance of working with Si" (Woodall's Rule, 1982), and "SiGe is not Si" (Woodall's Corollary, 1990). However, from the vantage of manufacturability, chips made of faster materials may offer better price-performance than nanoscaled Si chips as we approach THz applications.

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ACRONYMS

HBT: Heterojunction bipolar transistor.
MOSFET: Metal-oxide-semicon. field effect transistor
SOI: Si on insulator.
High-K: A material with a high dielectric constant, K.