Thermal Management of High Power Devices

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Abstract **- We report in this paper the thermal effects onto the performances of high power microwave transistors. Also, thermal simulation results along with means to optimize the heat dissipation on a wafer level are discussed. Finally we present a novel active thermal management technique using micro-fluidic channels. The simple fabrication process is presented.**

I. INTRODUCTION

Due to the tremendous evolution of the power densities in transistors, related to the continuous device miniaturzation, and the maturation of power technologies based on wide-bandgap semiconductors, conventionnal packaging techniques are not always suitable to dissipate the generated heat in devices. This results in parasitic effects that affect the circuit performances, reliability and lifetime [1-6].

The presence of thermal effects results from the incapacity of the system in which the IC is inserted (devices, board, interface board/device, package, and other fixtures) to drain enough heat away from the device's active region. Since every element of the system contributes to the overall heat flow, a careful investigation must be performed to identify the critical points that must be optimized.

We present in this paper the effects of self-heating onto the devices performances. Then, thermal simulation results are presented to highlight the different ways to optimize the thermal management on a wafer level. Finally we recall the conventional thermal management methods used in the micro-electronic industry before presenting a novel active cooling technique. This advanced thermal managing technique is based on strong local heat extraction using 3-D micro-fluidic channels fabricated near the IC's hot spots. The simple fabrication technique is presented.

II. THERMAL EFFECTS ON DEVICE PERFORMANCES

Under high power conditions, the device lattice temperature increases and so does the carrier phonon scattering rate, which leads to a drop in the carrier mobility. This effect has been reported to be of great influence in reducing all the device performances, as well as its reliability and lifetime. Biasing devices during a short period of time reduces carrier / lattice exchanges and therefore one can control the heat dissipation in the device. Fig.1 compares the measured f_T and transducer gain (G_T) versus V_{GS} obtained under pulsed and continuous mode of operation of a high power GaN-based transistor (W_G = 250µm, L_G = 0.35µm). The timing parameters used during the PW measurements are selected to overcome most of the self-heating effects in the device. It is noteworthy that under pulsed operation, the cutoff frequency increases by about 5% compared to the CW mode. Also, there is a 3dB improvement of the gain when the device operates in a heat-free environment.

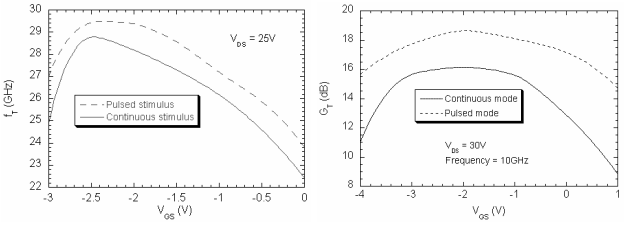


Fig. 1 Transfer characteristics of an AlGaN/GaN HFET (W_G=250µm, L_G=0.35µm) from 380K to 540K.

In addition, using an infra-red microscope it is possible to observe the evolution of the device peak surface temperature (T_{PEAK}) under microwave large-signal operation. Fig.2 shows the evolution of T_{PEAK} and of the total power to dissipate in the device (P_{DISS}) with the RF input power level (P_{IN}). The

tuning conditions of the power device were selected such that the test setup can drive the device into saturation while achieving maximum PAE. We observe that, T_{PEAK} and P_{DISS} varies with the RF input power level. In this example, P_{DISS} varies between 2.8W and 2.3W leading to a relative variation of around 20%. As expected, the peak surface temperature strictly follows the trend of variation of the parameter P_{DISS}, and varies from 134ºC to 124ºC resulting in a relative variation of the device surface peak temperature on the order of 10%. This variation of the device temperature is associated to the variation of the power to dissipate and thus of the magnitude of the thermal effect. It results in a change in the device transport properties and device performances, highlighting the importance of reducing self-heating effects to achieve a simple microwave device model.

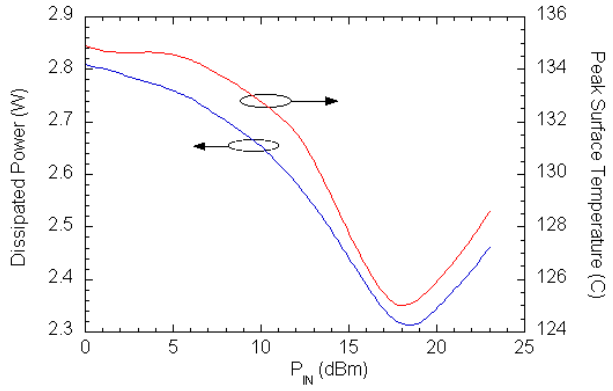
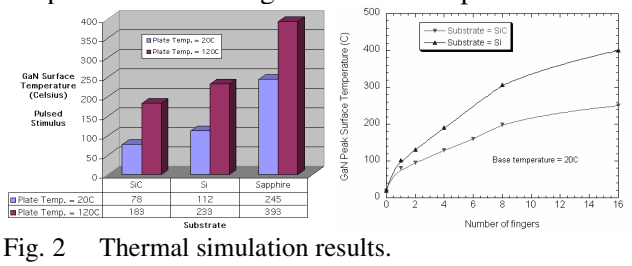


Fig. 2 Evolution of the peak surface temperature with the RF input power level.

III. Thermal Analysis on a Wafer Level

Thermal simulations are performed under continuous wave in order to identify the parameters that control the temperature distribution in devices. Fig.2 illustrates the impacts of the substrate type and of the number of fingers onto the peak channel temperature of a 2-finger AlGaN/GaN power HFET.



	SiC	Si	Sapphire
Plate Temp. = 20C	78	112	245
Plate Temp. = 120C	188	233	393

Fig. 2 Thermal simulation results.

As expected, technological parameters such the substrate type and substrate thickness, as well as device geometrical parameters (number of fingers, gate pitch…) strongly impacts the transistors channel temperature.

Trying to reduce the thermal effects present in a device by improving the heat dissipation through the selection of appropriate materials and device designs is a very natural approach, however, one may also question the role of the circuit design on the self-heating. The PAE plays a significant role in thermal effects because it controls the total power to dissipate in the device; and when designing a power amplifier (PA), the input and output matching networks are implemented to optimize the transistor for a certain behavior. Therefore the performance of a PA in term of PAE can be improved by including harmonic tuning in the design of the matching networks: increasing the complexity of the circuit design results in a reduction of the thermal effects.

IV. Conventional Thermal Management Techniques

Fig.2 shows the main elements that contribute to the heat flow of a FET in a conventional and in a flip-chip configuration. The heat spreads from the device channel, vertically in the different layers, and horizontally through the layers.

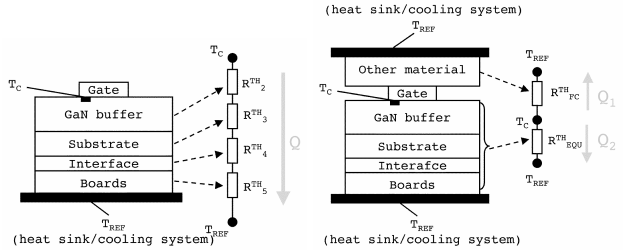


Fig. 2 Transfer characteristics of an AlGaN/GaN HFET (W_G=250µm, L_G=0.35µm) from 380K to 540K.

In a conventional configuration the channel temperature can be approximated by:

$$T_C = Q \cdot \left(\sum R_i^{TH}\right) + T_{REF} \quad (1)$$

And, in a flip-chip configuration, the channel temperature can be approximated by:

$$T_C = Q_1 \cdot R_{FC}^{TH} + T_{REF} = Q_2 \cdot R_{EQU}^{TH} + T_{REF} \quad (2)$$

Where R^{TH}_i is the thermal resistance associated to each layer, T_{REF} is the reference temperature fixed by the environment or a cooling system, T_C is the channel temperature, and Q_i represents the heat flow from the device channel to the reference temperature.

Similar considerations can be established when an IC is packaged. In any case, the basic solution to drain maximum heat away from the active region is

to reduce the thermal resistances and/or to reduce the temperature of the environment.

Additionally, cooling techniques may be used. They can be divided into two categories: the air cooled techniques and the compact heat exchanger techniques. The first technique is based on the passive dissipation of the heat using optimized heat sink and airflow. The second one is based on the circulation of a fluid that drains the heat away from the IC, the fluid being cooled down through the use of compact heat exchangers.

V. An Advanced Thermal Management Technique

In this section we present a tri-dimensional micro-channel technology for System-On-Package micro-fluidic micro-system that enables local active cooling. The idea is a strong local heat extraction using 3-D micro-fluidic channels fabricated near the IC's hot spots.

Similar devices have been previously made by injection molding (IM) and hot embossing in the context of miniaturized systems for biochemical analysis and nano-sensor devices for these systems. However three dimensional micro-channel networks are still very challenging to realize and solutions proposed to date are not cost effective. It is clear that the conception and the fabrication of new generation multi-functional nano-fluidic-electronical nano-systems require the development of new technologies.

The three dimensionnal micro-channel network proposed in this paper has been realized on silicon wafer with SU-8 epoxy. The maximum temperature during the fabrication is 95°C, so it can been directly built on sensitive elements. The structures are totally transparent and realized by photolithography with micronic accuracy. No mechanical alignment and no sacrificial layer etching are required. This approach offers large degrees of freedom for the conception and the design of true three-dimensional micro-channel network.

Figure 1 shows a cross section of the prototype. The total thickness is 130 µm. The micro-channel dimensions vary on a wide range from 40 µm to 500 µm width (Fig. 1), for a depth of 45 µm. Vias diameter vary from 40 μm^2 to 500 $\mu m.^2$(Fig. 2).

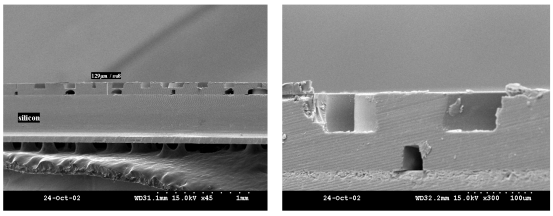


Fig. 3 Tri-dimensional micro-channel network cross-section view, and Stacked micro-channel detailed view.

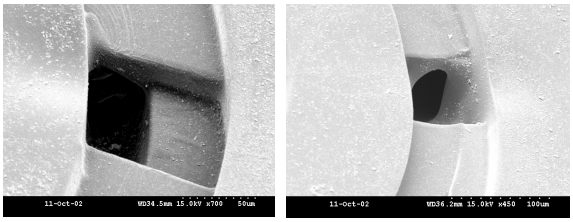


Fig. 3 Vertical vias detailled views. (80 μm^2).

VI. Conclusion

Due to the tremendous evolution of the power densities in transistors and ICs thermal management is a serious issue. We have first reported in this paper the thermal effects onto the performances of high power microwave transistors in order to quantify the magnitude of the thermal effects. Then, we present thermal simulation results with means to optimize the heat dissipation on a wafer level. Finally we have presented a novel active thermal management technique using micro-fluidic channels, along with their simple fabrication process.

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ACRONYMS

IC: Integrated Circuits
f_T: Cutoff Frequency
G_T: Transducer Gain
V_{GS}: Gate-to-Source Voltage
W_G: Gate Width
L_G: Gate Length
PW: Pulsed Wave
CW: Continuous Wave
T_{PEAK}: Peak Temperature
P_{DISS}: Dissipated Power
P_{IN}: Input Power
PAE: Power Added Efficiency
HFET: Hetero-junction Field Effect Transistor
PA: Power Amplifier
FET: Filed Effect Transistor
T_C: Channel Temperature
R_{TH}: Thermal Resistance
T_{REF}: Reference Temperature
Q_i: Heat Flow
IM: Injection Molding